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Growth of semiconductor (core) / functional oxide (shell) nanowires: application to photoelectrochemical water splitting

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Introduction

Since 2004 when L. Samuelson group accomplished the epitaxial growth of III-V semiconductor nanowires (NWs) on silicon wafer,[1] the integration of 1 dimentional (1D) nanoscale III-V semiconductor with the well-developed Si industry turned to be one of the most promising hybrid systems for optoelectronics. Maintaining NW's 1D feature, there are two ways to construct heterosystems with other kinds of materials, namely the axial heterostructure and the radial one (core / shell NWs). It is hence possible to use NWs to make complex nanostructures with improved physical properties. Compared to the axial one, the radial heterostructure has higher tolerance to surface effects. Besides, the core / shell geometry provides an orthogonalization of the charge and light pathways and thus yields an efficient carrier collection, which is pursued by all the photoelectric devices.

So far, most of the published works on semiconductor core / shell NWs concern semiconductors of the same family. The fabrication of highly heterogeneous shell, such as functional oxides or metals, on III-V semiconducting NWs is still of great challenge. One of the difficulties arises from the *ex-situ* growth procedure of the heterogeneous shell: the sample transfer among different separate reactors is not under ultra-high vacuum (UHV) conditions; hence, during the transfer, the III-V NW facets suffer an uncontrolled oxidation and / or contamination. Thorough studies about the oxidation and the corresponding effect on the following shell growth as well as the property of the final heterostructure is still missing. A contamination-free and reversible surface protection would be rather important for the future application design. Recently, the integration of heterogeneous materials such as silicon,[2] silicide[3] or metals[4] on GaAs NWs has been achieved, opening the way to the fabrication of original devices. As well known, perovskite oxides possess a wide range of properties, such as piezoelectricity, ferroelectricity *etc.*, which are complementary to those of semiconductors. This combination can thus facilitate the development of multifunctional devices. So the method to accomplish the epitaxial growth of perovskite oxides on III-V NWs is of great necessary. However, the combination with functional oxides of perovskite structure is still on the thin film level, even though it is theoretically possible to epitaxially grow this kind of materials on semiconductors like Si and GaAs for a small lattice mismatch. Furthermore, since perovskite oxides have notably similar crystallographic structure, stacking different ones layer by layer is rather operational, which means a general method might be possible for different kinds of perovskite oxides and a multifunctional device based on core-multishell NW array could be as well feasible.

These semiconductor core / oxide shell NWs could be promising for a wide range of applications including the photoelectrochemical water splitting. The photoelectrochemical (PEC) hydrogen production from water provides a way to directly convert solar energy into a

storable clean fuel. The tandem structure combined with semiconductors with different band gaps can improve the solar spectrum absorption. It is reported that a 1.7 eV / 1.1 eV band gap tandem structure would produce optimal energy-conversion efficiencies that are comparable to those of commercial triple-junction cells.[5] Several compounds that satisfy the requirement of the 1.7 eV band gap can be obtained by adjusting the composition of the ternary and quaternary III-V semiconductors. GaAs NW array can serve as a model system to demonstrate the quality of NW-array light absorbers enabled by the III-V NW-on-Si strategy. However, one of the primary problems, which prevents such narrow band gap materials from being utilized as photocatalysts, is that their surfaces are photochemically unstable in the electrolyte. Furthermore, NWs configuration offers a large surface area, enhancing the light absorption while increasing surface recombination possibility as more surface states are introduced. L. Ji *et al.* reported a Si-based photocathode with an epitaxial $SrTiO_3$ layer working as a photocathode for PEC cells.[6] Monocrystalline $SrTiO_3$ was epitaxially grown on Si with a very low interface state density.[7] Photogenerated electrons can be transported easily through the $SrTiO_3$ / Si junction because of the perfect structure and the good conduction band alignment. Taking into the consideration of the structure similarity between Si and GaAs, $SrTiO_3$ could be integrated with GaAs NWs as a passivation layer for water splitting, showing more benefit of the combination between III-V semiconductors and pervoskite oxides.

In this PhD work, we aimed at developing the growth of GaAs (core) / functional oxide (shell) NW arrays on Si substrates for photoelectrochemical water splitting. There are six chapters in total. The main topic for each chapter is listed as following:

Chapter 1: The background and the challenges are presented for the fabrication of III-V semiconductor (core) / oxide (shell) NW arrays. The advantages and difficulties of such heterogeneous systems are also introduced when they are applied to photoelectrochemical devices. The fundamental knowledge of molecular beam epitaxy and photoelectrochemistry is referred to be comprehensible.

Chapter 2: This chapter is dedicated to present the main experimental techniques which were used during the PhD study. The basic theories of these techniques are introduced, as well as some common problems we met during the practical work.

Chapter3: We investigated the effect of different experimental parameters on the morphology of the GaAs NW arrays obtained by the self-catalyzed MBE growth. This first experimental chapter gives a fundamental understanding of the growth mechanism of GaAs NWs on Si substrate, and also offers a relatively practical guideline for who plans to control the NW morphology.

Chapter 4: In this chapter, we systematically studied the surface oxidation of GaAs NWs and its negative effect on the subsequent shell growth. Then, the efficiency of the As-cap method against the oxidation and contamination was investigated.

Chapter 5: We investigated the growth of a $SrTiO_3$ shell on self-catalyzed GaAs NWs grown by VLS assisted MBE on Si(111) substrates. RHEED, SEM, TEM and XPS measurements were performed to determine the structural, morphological and chemical properties of the core / shell NW arrays. It was shown that most of the perovskite structure $SrTiO_3$ shell appears to be oriented with respect to the GaAs lattice, presenting the possibility to integrate monocrystalline perovskite oxides on GaAs NWs.

Chapter 6: This chapter contains the work on the GaAs NWs-based PEC cells. To enhance the cell performance, the geometry of NWs was optimised. The effect of doping concentration was then studied. To avoid the degradation of electrodes caused by the photocorrosion of GaAs NWs, an oxide passivation layer was applied. GaAs / $SrTiO_3$ NWs were firstly used for the realization of a PEC cell for water splitting. Then, GaAs / TiO_2 NWs were grown too as the PEC photoelectrode. Pt particles as co-catalyst, was finally studied as the last part of the work.

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Contents

Chapter 1. GaAs based core / oxide shell NWs on silicon substrate: a promising heterogeneous system for the photoelectrochemical cells

1. III-V semiconductor nanowires (NWs) on Si substrate

III-V Semiconductor NWs have received much attention as a new class of materials with remarkable potentials for combining both advantages of III-V semiconductors (direct bandgap, high carrier mobility, and advanced band-structure engineering *etc.*) with those of the nanoscale 1D geometry (free-standing nature and pronounced quantum confinement effects).[1] The epitaxial growth of III-V NWs on silicon (Si) wafer hasn't been accomplished until 2004 by L. Samuelson group.[2] The successive integration with the well-developed Si industry and the possibility to construct more complex geometries endow III-V NWs a rather bright future.

In the semiconductor-based device domain, Si is the most important material due to the fact that Si can be large-scale produced with extremely high monocrystalline quality and purity at low cost. One of the few disadvantages of Si is its indirect bandgap, which causes inefficient light absorption and weak light emission. GaAs is the prototype of most III-V compound semiconductors, providing a very efficient electron-light coupling thanks to its direct bandgap. This property is central to optoelectronic devices such as light-emitting diodes, laser diodes and high-efficiency solar cells.[3,4] It is hence very desirable to integrate GaAs with Si substrate to combine their respective advantages and then enhance the performances of devices. Except for its technological importance, the heteroepitaxy of GaAs (polar) on Si (non-polar) can also serve as a typical model system for the monolithic integration of polar on non-polar semiconductors.[5]

1.1. The advantages of this kind of heterogeneous system

Before the rise of semiconductor NWs, thin films had been the mainstream research topic in material science since the earlier achievement on its epitaxial growth on the Si substrate.[6-8] The as-required material, different from Si, is also referred to heteroepitaxial layer, or heteroepilayer. There are several factors that affect the structural quality of the heteroepilayer.

The first one is the lattice mismatch originated from the noticeable difference of crystal lattice parameters between the substrate and the heteroepilayer. Thin enough heteroepilayers can adopt the lattice constant of the substrate (pseudomorphic and

coherent growth) and stay strained. With the increase of the heteroepilayer thickness, the lattice stress / strain develops more or less quickly depending on the lattice mismatch, causing plastic relaxation defects as misfit dislocations and then threading dislocations dramatically affecting the performances of devices.

The second is the difference in thermal expansion coefficients of the two materials, resulting in their different behaviors when the heterostructure is cooled down from a relatively high temperature (growth temperature) to ambient conditions. The heteroepilayer will crack while the substrate bows and bends if the heteroepilayer thickness exceeds a critical value.

Anti-Phase Boundaries (APBs) is another factor. If we consider the 2D growth of a III-V layer on a Si substrate, APBs typically form at single atomic steps of the elemental Si surface, when the neighboring terraces are decorated by the identical compound.[9,10] The III-V neighboring terraces are configured in opposite order for the III and V planes and form an APB on either side of which the polarity of the III-V layer is inverted.

Several techniques have been implemented to suppress the dislocation defects in heterosystem as GaAs / Si, such as substrate misorientation and high-temperature surface annealing as well as two-steps growth procedures.[5,11,12] Besides these efforts made to reduce the dislocation density in the heteroepilayer, a different and relatively new solution arose: reducing one more dimension of the heteroepilayer to the nanometric size and constructing free standing NWs (Figure 1).

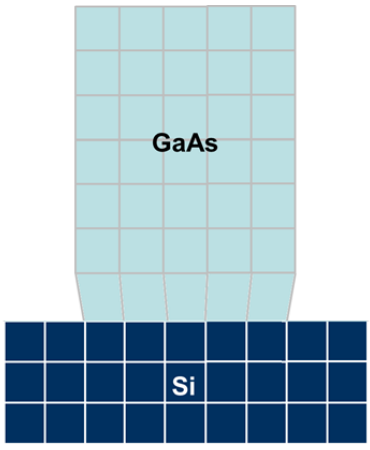

Figure 1. Schematic of a free standing GaAs NW on a Si substrate showing how the strain is released through elastic relaxation.

As the surface to volume ratio of planar layers is relatively small, materials in the shape of thin film are laterally constrained. In 1D NWs strain originating from the heterostructure interface can be relieved via elastic relaxation from NW lateral surfaces in the NW diameter is lower than a critical value which depends on the lattice mismatch.[13] Therefore, NWs offer

the possibility for obtaining strain- and defect-free crystals. A superior crystalline quality of NWs, largely independent from the substrate, is a major driving force for the NW concerning research.

1.2. Vapour-Liquid-Solid (VLS) method for the growth of GaAs NWs via molecular beam epitaxy (MBE)

1.2.1. Brief introduction of the VLS-MBE growth mode

The most widely used method to fabricate III-V semiconductor NWs by MBE is the VLS mechanism. The material source is heated in the emission cell attached to the MBE chamber to produce a vapour phase. Liquid particles on the substrate serve as the catalyst in order to obtain: 1) numerous isolated nucleations of NWs instead of a continuous 2D structure and 2) a strong anisotropy of the growth rate: fast growth in the NW axial direction and low rate for the radial direction to achieve the 1D geometry. The solid phase corresponds to the crystalline substrate (in the beginning of the growth) as well as the as-grown NWs (during the growth).

The whole VLS growth process can be describe as follow: 1) vapour growth species are concentrated into liquid metal droplets acting as a reservoir for the growth species; 2) growth species will combine and nucleate on the solid surface if the metal droplets reach supersaturation; and 3) the droplets will be lifted up because of the material growth at the liquid-solid interface. It should be noted that the growth species incorporated in the droplet come from the direct impingement as well as by surface diffusion from nearby surfaces (*e.g.* substrate surface and NW lateral surface).

For III-V semiconductors, the two most common crystal structures are the cubic one termed as Zinc Blende (ZB) and the other hexagonal Wurtzite (WZ) structure. WZ insertions are usually found in the ZB III-V NWs, and vice versa. Since the coexistence of two phases impedes fundamental studies as well as the improvement of device performances, phase purity control is one of the main challenges of III-V NW fabrication. Hence the nucleation during the VLS process is well studied.

The most adapted growth model is the one proposed by F. Glas *et al.* for gold-catalyzed III-V NWs.[14] It is assumed that the nucleation must occur at the solid-liquid interface. There are two possible nucleation sites, one is completely inside the liquid phase (Figure 2 a), the other one is at the triple phase line (TPL, Figure 2 b). Supposing that the height of the solid epitaxial 2D island nucleus is h, its perimeter is P, the upper surface area is indexed as A and the substrate is of ZB structure. In the former case, a change of free enthalpy after a nucleus is formed entirely inside the droplet can be expressed as follow:

$$\Delta G(0) = -Ah\Delta\mu + Ph\gamma_{IL} + A(\gamma_{NL} - \gamma_{SL} + \gamma_{SN})$$

where $\Delta\mu$ is the difference of chemical potential for the III-V pairs in liquid and solid phases; γ_{lL} is the energy per unit area of the lateral interface between nucleus and liquid; γ_{NL}, γ_{SL} and γ_{SN} are the energies per unit area of the upper nucleus-liquid interfaces, substrate-liquid and substrate-nucleus, respectively (Figure 2 a). For the first case with the nucleus completely inside the liquid phase, γ_{NL} is always equal to γ_{SL}, and γ_{lL} is identical for both ZB and WZ. However, γ_{SN} depends on the surface orientation of nucleus and that of the solid phase (ZB). If the orientation is the same (ZB-ZB), $\gamma_{SN} = 0$; if not (WZ-ZB), $\gamma_{SN} > 0$. Therefore, $\Delta G^{WZ} - \Delta G^{ZB} = A\gamma_{SN} > 0$, which means the ZB structure is preferred.

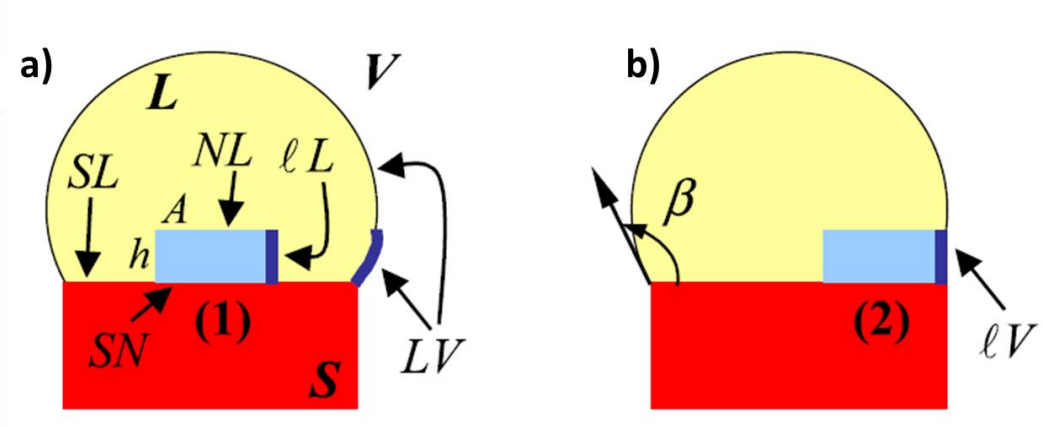

Figure 2. a) Nucleus at the nanowire-liquid interface, with interfaces of interest. b) Transferring the nucleus to the triple phase line eliminates and creates interfacial areas, indicated by thick lines in, respectively, a) and b).[14]

For the second case with the nucleus at TPL, part of the nucleus will contact with the vapour phase as shown in Figure 2 b. The corresponding interface energy is referred to γ_{lV}. It is assumed that the volume of the droplet is identical in both cases, therefore part of the liquid-vapor interface area (τs) is replaced by the nucleus-vapour interface (s). α is the fraction of the island perimeter contacting with the vapour, α=0 means that the nucleus is completely inside the droplet, case one. The formation enthalpy of the nucleus at the triple phase is:

$$\Delta G(\alpha) = -Ah\Delta\mu + Ph[(1-\alpha)\gamma_{lL} + \alpha(\gamma_{lV} - \tau\gamma_{LV})] + A\gamma_{SN}$$

So for a given nucleus, the difference in formation enthalpies between case one and two is:

$$\Delta G(\alpha) - \Delta G(0) = \alpha Ph(\gamma_{lV} - \gamma_{lL} - \tau\gamma_{LV})$$

The contact angle ϕ between droplet and the front of NW is used to estimate τ ($\tau = sin\phi$). So if $\gamma_{lV} - \gamma_{lL} - \gamma_{LV} sin\phi < 0$, the nucleation at the triple phase line is favourable. Then by assuming $\gamma_{lL} \approx \tau\gamma_{lV}$ and $90° < \phi < 125°$ (from experimental data) leading to $sin\phi > 0.82$, it is argued that the above inequality is safely satisfied and thus the nuclei should always form at TPL. Then, considering the relative orientation of a given nucleus and a

certain edge, it is possible to know the preferable structure. It is thus demonstrated that WZ structure is the more feasible when nucleation occurs at the triple phase and if the III-V supersaturation in the droplet is higher than a critical value. It is worth noting that this fundamental model is still well adapted for the self-catalyzed NW growth and keeps offering the inspiration for newer and more accurate models on the basis of experimental results obtained via more developed characterization methods such as the *in-situ* transmission electron microscopy (TEM).[15]

1.1.1. Foreign metal catalyzed III-V NWs

Nanoparticle seeds which are not the component of NWs are referred as foreign metals seed. The most obvious advantage of foreign metal seeded VLS mode is that the growth of NWs is less sensitive to changes of experimental parameters, since the seed particle volume is in principle fixed.[1] The parameter (*e.g*. temperature, flux ratio between V and III elements) window is thus evidently broadened compared to the self seeded process (discussed later), which in turn offers a greater freedom for NW morphology design. For III-V NWs grown by MBE, nickel,[16] palladium,[17] manganese[18] catalysts have been reported. However, the most used foreign metal seed is gold.[19-21]

The foreign metal seeded method lost its interest gradually when implemented in the device fabrication, in spite of the important advances and impressive early results obtained by. This is ascribed to foreign element itself as a factor complicating the system and an unintentional contamination. Among the aforementioned metals, the gold seed has given rise to the strongest opposing voices. On the one hand, using gold, one of the noble metals, is indeed against the cost-down principle in the device upscaling process. On the other hand, the performance of the practical devices can be degraded because the Au serving as the semiconductor dopant[22,23] or because Au impurities must be avoided in CMOS (complementary metal-oxide-semiconductor) process lines.

1.2.2. Self-catalyzed III-V NWs

If the seed particle is made of one of the NW components, the VLS process is named as self-catalyzed growth, opposite to the foreign seeded one. Self-catalyzed NW growth can offer obvious advantages in terms of simplicity and cleanliness for the fabrication process comparing to the foreign seeded one. For III-V NWs, group III metallic elements with low melting temperature always serve as the catalyst. Since the constituent of catalyst is also the growth source of NWs, the droplet can be gradually consumed. The contact angle is in turn changed, impacting the NW morphology and structure. Thus, self-catalyzed growth is more sensitive to the growth parameters like growth temperature, V / III flux ratio *etc*.[24,25] By tuning the growth temperature and V / III ratio, essentially to control the dynamic balance between consumption and feeding of group III species in the droplets as well as the droplet contact angle, NW's morphology and crystal structure can be "manipulated" to fabricate more complex nanostructures.

In the scope of this work, Ga-catalyzed GaAs NWs are most concerned. The understanding of this growth mechanism owes to the pioneering works done by A. Fontcuberta i Morral *et al.*[26] Figure 3 depicts a schematic of one GaAs NW grown via a Ga-catalyzed process on a Si(111) substrate covered by a thin SiO_2 or SiO_x layer. Ga and As can be both provided in the beginning of the growth at 600 °C, Ga forms the catalyst droplets while As desorbs or Ga can be deposited before the As supply, termed as pre-deposition[27] (case shown in Figure 3). The Ga droplets react with oxide layer according to the following equations:[28]

$$SiO_2 + 4Ga \rightarrow Si + 2Ga_2O \quad (1\text{-}1)$$

$$SiO_2 + Si \rightarrow 2SiO \quad (1\text{-}2)$$

or

$$SiO_2 + 2Ga \rightarrow SiO + Ga_2O \quad (2)$$

Ga_2O and SiO oxides are assumed to be desorbed at 600 ° C with the formation of pinholes in the oxide layer leading to a contact between the Ga droplets and Si. Once these droplets are formed, enrichment and supersaturation of Ga droplets with As leads to the nucleation of GaAs at the liquid-solid interface and to the growth of the GaAs NWs. It has been shown recently that the oxide thickness and composition and the Ga droplet size are crucial parameters to lead to vertical GaAs NWs on Si(111) substrate.[25]

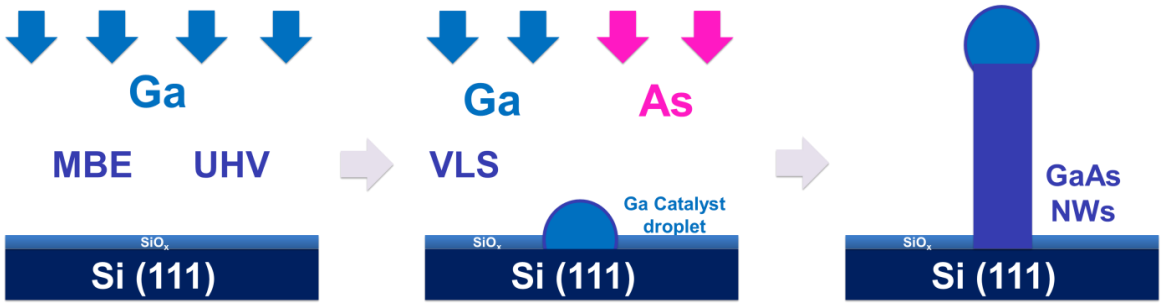

Figure 3. Schematic of the self-catalyzed growth of GaAs NWs by MBE on a Si(111) substrate recovered by a thin oxide layer.

2. III-V-Core / shell NWs

As we mentioned before, it is quite feasible to use NWs to make more complex nanostructures. There are two ways to construct heterosystem with other kinds of materials, namely the axial heterostructure and the radial one. The corresponding schematics are displayed in Figure 4. The axial heterostructure shows a flexibility in the structural design and has a higher tolerance to doping variations.[29] However, the theoretical study made by N. Huang *et al.* indicates that axial heterojunctions are rather sensitive to surface states.[30]

Comparing to the axial one, the radial heterostructure has higher tolerances to surface effects,[29,31] but shows higher sensitivity to the strain in an epitaxial hybrid heterostructure. Besides, the core / shell geometry provides an orthogonalization of the charges and light pathways and thus yields an efficient carrier collection,[32,33] purposely pursued by all the photoelectric devices.

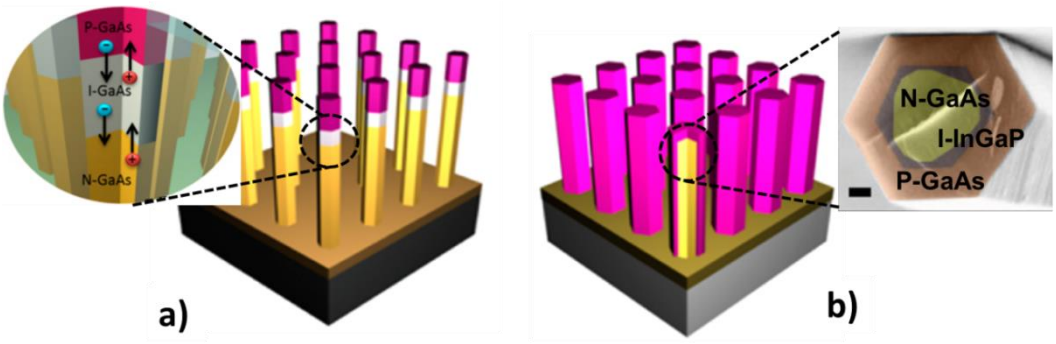

Figure 4. Comparison between NWs based on: a) an axial heterostrucutre and b) a radial heterostructure.[29]

2.1. Heterogeneity in core / shell NWs

Using III-V semiconductor NWs as core, the shell materials are commonly made by the structurally similar III-V compound semiconductors for the mechanochemical matching feature. It makes it more popular for the simple *in-situ* manipulation of the shell chemical composition as well as the doping concentration in MBE chamber. For a GaAs NW core, GaP,[34] AlGaAs,[3,35,36] GaAsP,[37,38] InGaP,[33,39] GaAsBi,[40] MnGaAs[41,42] *etc*. have been used as the shell material. These as-prepared core / shell NWs show a great potential in devices like light emitting diodes, transistors, solar cells and so on.[4,43,44]

The growth of metals on III-V semiconductor NWs has been relatively unexplored compared to the case of growth on a 2D substrate. In most cases, the metallic shell is rough and has no apparent texture as observed in the GaN / Fe[45] or GaAs / Ni[46] systems. An abrupt epitaxial interface was realized in the InAs / Al system by P. Krogstrup *et al*.[47] The direct growth of an epitaxied silicide (Fe_3Si) was carried out on GaAs NWs.[48-50]

It is more complicated to construct III-V / IV hybrid NWs due to the lattice mismatching. As known, the small footprint of NWs enables the epitaxial fabrication of highly lattice-mismatched III-V NWs on a IV substrate. In principle, NWs should also present an effective strain relaxation for a III-V / IV core / shell NW.[51] It is now accepted that the formation of misfit dislocations depends both on the lattice mismatch and the relative dimensions of the core and the shell.[52] R. Algra *et al*. is the first group who constructed a III-V / IV core / shell hybrid system with GaP serving as the core and Si as the shell.[53] The crystalline structure of the GaP core was successfully transferred to the Si shell. Figure 5 illustrates results obtained

later by the same group on the epitaxial growth of a Si shell on ZB GaAs NWs and on WZ GaP NWs.[54,55] It is shown that Si adopts the cubic and the hexagonal crystal structure of the III-V core, respectively (Figure 5). The same observation has been obtained for ZB GaAs / Si NWs synthesized by S. Conesa-Boj *et al*. by combining MBE with plasma enhanced chemical vapor deposition (PECVD).[56]

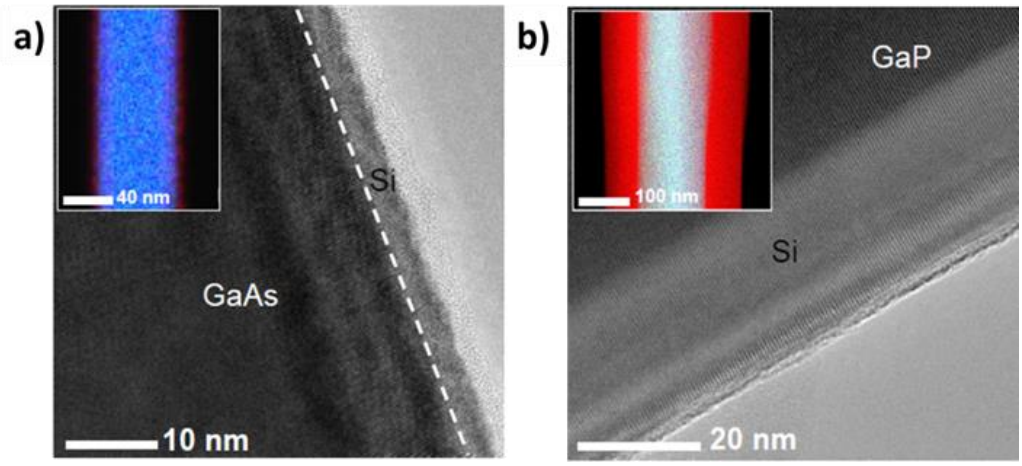

Figure 5. a) GaAs / Si and b) GaP / Si core / shell NWs and their corresponding elemental distribution map. Si component is marked in red.[55]

Another category of shell is made of functional oxides, displaying advantageous electric, thermal, and magnetic properties which most of semiconductors don't possess. The coupling of III-V semiconductor with functional oxides is definitely beneficial to the multifunctional devices. Nevertheless, the high lattice mismatch and strong chemical heterogeneity hamper the development of such hybrid structures. There is thus few epitaxial III-V semiconductor / oxide core / shell NWs related study reported. Researchers still see the possibility and potential of this kind of hybrid NWs from the successful combination between perovskite oxides and III-V semiconductors in 2D form.[57-60] Further, oxides, even in the amorphous state, present good properties for practical devices.[61] F. Ishikawa *et al.* reported the synthesis of GaAs / amorphous $AlGaO_x$, by the selective oxidation of GaAs / AlGaAs core / shell NWs, exhibiting a good luminescence over the entire visible wavelength range.[61,62] Amorphous TiO_2 is also used as the shell against the photocorrosion suffered by the relatively vulnerable III-V semiconductor electrode during water splitting test.[63]

2.2. Heterostructure interface

Practical devices, such as transistors, lasers, and solar cells, are sensitive to interfacial phenomena. Interfaces play an important role in data processing, memory, electronic communication *etc*.[64] One of the key challenges in semiconductor-based heterostructure design is to realise a defect free interface in order to decrease the surface recombination velocity.[65,66]

The lattice and structure mismatch between the two components causes strains which create crystal defects strongly impeding the homogeneous shell growth. These defects can also act as trap states for charge carriers.[67,68] For both MgO / GaAs and SiO_2 / GaAs heterosytems, the Fermi level is pinned at GaAs midgap, displaying no improvement in photoluminescence (PL) intensity comparing to that of the bare GaAs.[65] The interface also should be abrupt and clean, the increasing of interfacial roughness will also degrade the carrier mobility.[69] Then, for heterostructures with high-k dielectric oxides, interface might be oxidized due to oxygen diffusion affecting the device performances.[69]

Many methods, including thermal, anodic, photochemical and plasma, are applied prior to the outer layer deposition for obtaining the ideal hybrid structure with sharp interface,[65] even though interface defects are difficult to completely repel and interface contaminations are easily introduced. Among them, the simplest one is the rapid thermal annealing (RTA) process (Figure 6 a).[70] However, for a compound semiconductor, RTA is less suitable. Taking III-V NWs as an example, the high temperature causes a higher loss of group V elements from the surfaces, resulting in the surface decomposition and the formation of group III-consisted clusters.[61] The atomic hydrogen etching is also very common (Figure 6 b).[56] But the surface oxidation will quickly happen if the etching machine doesn't connect to the other deposition reactor under vacuum. The most adaptable method for MBE grown III-V NWs should be the deposition of an arsenic (As) capping layer which is then sublimed at a low temperature (typically 350 °C) in the deposition reactor (Figure 6 c).[71,72] Nevertheless, there was no systematic study on the effect and efficiency of this method before I stated my PhD. More efforts should be put to the optimization of the interface structure in order to synthesis the ideal core / shell hybrid NWs and to enhance the corresponding devices performances.

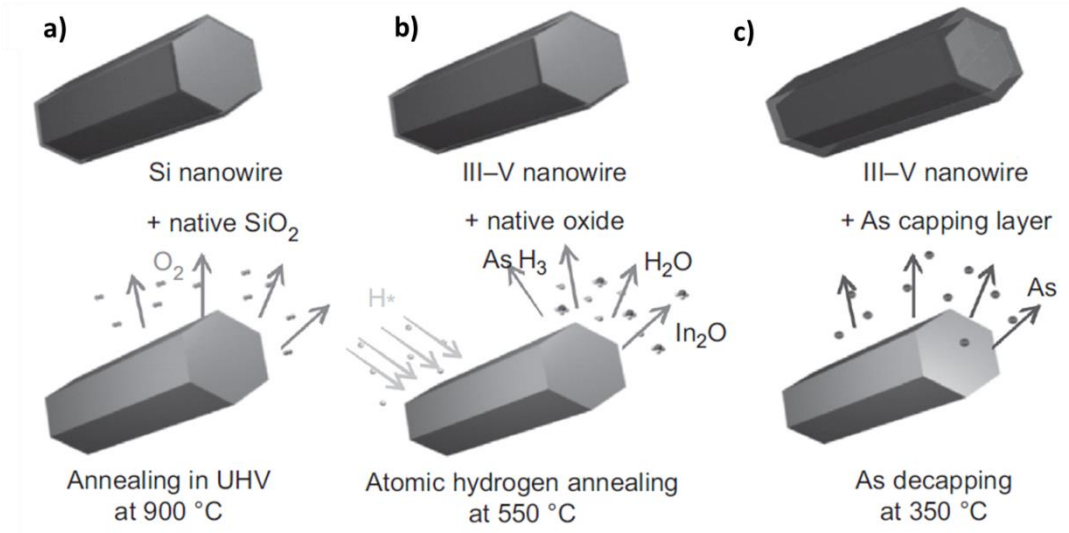

Figure 6. Different NW surface treatments:[71] a) RTA, b) atomic hydrogen etching, c) sublimation of an As capping layer.

In summary, the III-V semiconductor (core) / functional oxides (shell) is of great interest for coupling the property of both core and shell materials to fabricate multifunctional devices. However, the difference between their crystal structure and the difficulty to control the interface structure hamper the development of this kind of heterosystem. An efficient method is needed for protecting the core surface from the contamination and oxidation and improving the interface quality as combining the shell. Then the combination between III-V semiconductors and oxides should be thoroughly studied to realise a good heterostructure and enhance its physical performance. Since the ecological and energetical problems nag people seriously, the eco-friend energy harvesting becomes one of the most important subject, such as water splitting to what the III-V semiconductor (core) / oxides (shell) NWs can be well applied. The fundamental of photoelectrochemical water splitting is discussed in the following section.

3. Semiconducting NWs for water splitting

3.1. Principles of photoelectrochemical (PEC) cells for water splitting

Fundamental principles of semiconductor electrochemistry were established during 1970s. But many important discoveries did not occur until the 1990s, as interest in renewable energies reinvigorated the field. A simplified schematic of PEC cell is shown in Figure 7.[73] The working electrode (illuminated) is made of a p-type semiconductor as photocathode, and a counter electrode serving as photoanode. For the water splitting by PEC cells, two half-reactions occur: the oxygen evolution reation (OER) which involves an electron transfer from the electrolyte to the photoanode (or a hole transfer from the photoanode to the electrolyte) and produces O_2, and the hydrogen evolution reaction (HER) which involves an electron transfer from the photocathode to the electrolyte (or a hole

transfer from the electrolyte to the photocathode) and produces H_2. The external circuit in PEC cells lowers the specifications of photoelectrodes which only have to meet the requirements of HER or OER.[74] This allows a wider choice of materials and architectures, hence a lower cost. Since HER and OER happen to two separated electrodes, it facilitates the gas separation and collection. The potential difference between water oxidation and reduction is 1.23 eV, which is also the minimum limit of the required band gap for a semiconductor-based photoelectrode. The core issue of PEC cells is to understand how the matter and charge are transferred through the semiconductor-electrolyte interface. The interface between the semiconductor and electrolyte is similar to semiconductor-metal and metal-electrolyte interfaces, which make it easier to understand.

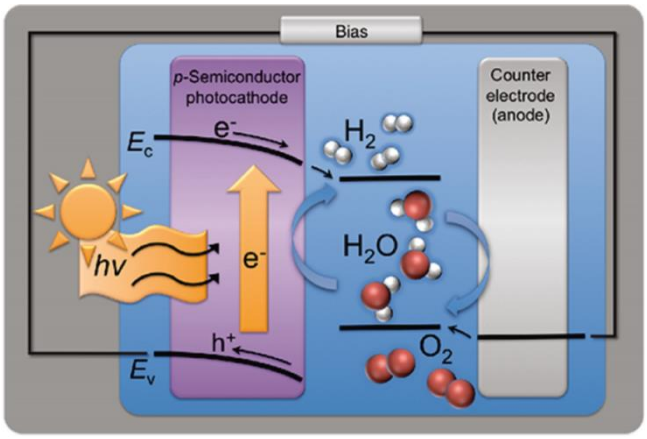

Figure 7. Schematic of a PEC cell with p-type semiconductor as photocathode (© 2011 Society of Photo-Optical Instrumentation Engineers (SPIE)).[73]

3.1.1. Quasi Fermi level and semiconductor / electrolyte junction under illumination

Semiconductors absorb photons with energy higher than or equal to its band gap, causing an excitation of electrons from the valence band (VB) to the conduction band (CB). Carrier recombinations occur simultaneously via the band to band transfer, Auger processes or at defect states, either in the bulk or at the surface of the semiconductor. The recombination process determines the minority carrier lifetime, τ_{min}. Hence, the hole and the electron concentrations depend on the rates at which excitonic pairs are photogenerated and removed. For a semiconductor under a steady illumination without applied bias, the excitation of electron-hole pair balances with their recombination. The concentrations of excess carriers (compared to the dark situation), Δn and Δp are equal.

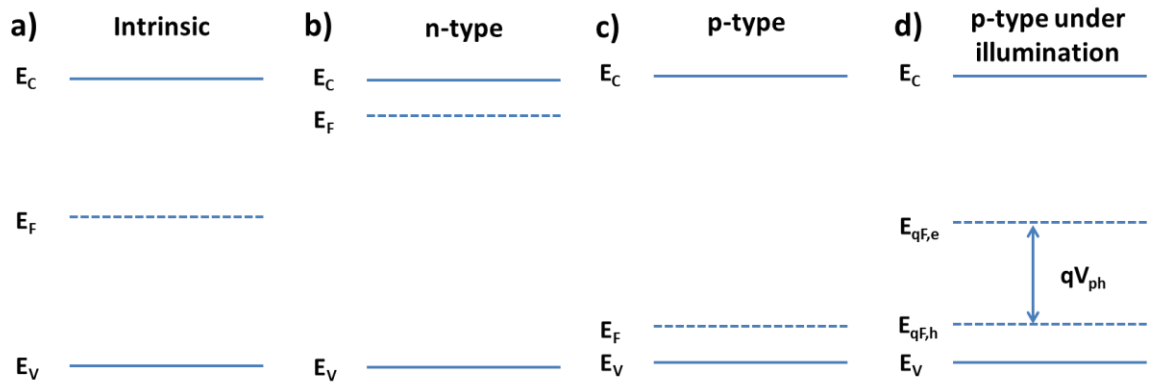

Figure 8. a-c) Band diagrams of intrinsic, n-type and p-type semiconductors, and their corresponding E_F; d) Fermi level splitting of the p-type semiconductor under illumination ($E_{qF,e}$ is strongly affected, whereas $E_{qF,h}$ remains essentially the same).

Taking the p-type semiconductor as an example, with and without illumination the change of majority carrier (hole) concentration is almost negligible ($p \gg \Delta p$), while the minority carrier (electron) concentration increases dramatically. It is a rather rapid process that photogenerated electrons and holes equilibrate with lattice phonons (in less than 10^{-12} s), whereas the recombination takes longer.[75] The distribution of thermally relaxed electrons and holes is thus described by quasi-Fermi energies $E_{qF,e}$ and $E_{qF,h}$, respectively. $E_{qF,h}$ keeps almost the same position as the original Fermi level (E_F) of the same p-type semiconductor without illumination (Figure 8 c, d) since the majority carrier concentration is approximate a constant ($p \gg \Delta p$). The energy splitting between $E_{qF,h}$ and $E_{qF,e}$ represents the free energy stored in the electron-hole pair which is the sum of their chemical potentials μ_{eh}:

$$\mu_{eh} = \mu_e + \mu_h = E_{qF,e} - E_{qF,h}$$

where μ_e and μ_h are the chemical potential of electrons and holes, respectively.

To extract the largest possible fraction of the stored energy is the main objective of energy conversion devices based on the semiconductor light absorption. This energy is converted to the electrical power for a solar cell and to the chemical product as H_2 for a PEC cell. The potential difference between $E_{qF,e}$ and $E_{qF,h}$ is also termed as photovoltage (V_{ph}, Figure 8 d). If only the illumination is responsible for breaking the system equilibrium, V_{ph} corresponds to the open circuit potential (V_{OC}).[76]

When the semiconductor contacts with a redox pair in the electrolyte under dark, a quasi equilibrium should be reached. The p-type semiconductor is used as an example again. As a reference, Figure 9 a describes the equilibrium state for a semiconductor under open circuit conditions (zero applied bias) without illumination. There is no net current, which means that the reduction of water (in this case) doesn't happen. Figure 9 b and c display the magnitude of the V_{ph} under different illumination intensities, where V_{ph} is dependent on the illumination intensity.[77] A higher photon flux brings more minority carriers and hence a

larger of Fermi level splitting. The band bending also decreases with the increase of illumination intensity. $E_{F,redox}$ is the Fermi energy of a given redox pair in the electrolyte, discussed in the following section.

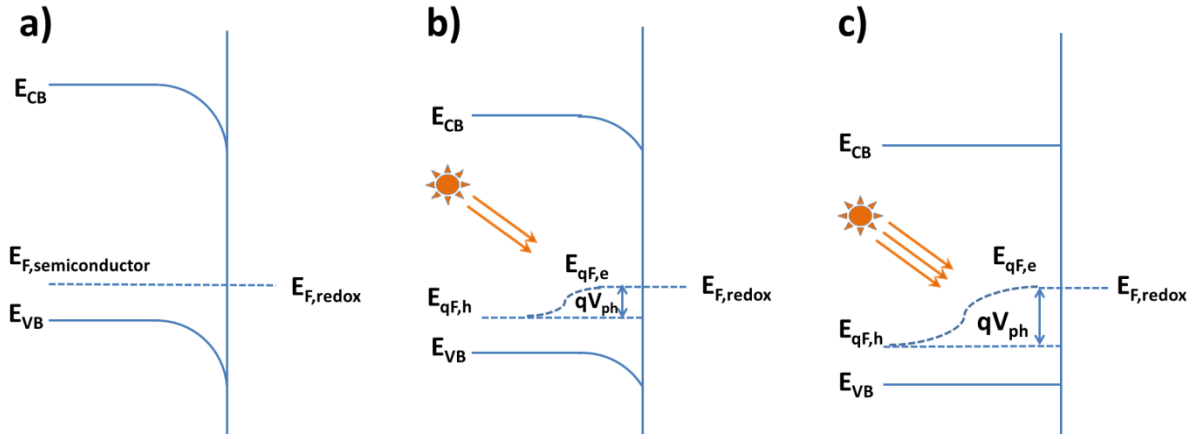

Figure 9. Schematic of Fermi level splitting caused by illumination for a p-type semiconductor uses as photocathode under the equilibrium situation at zero applied bias: a) in the dark, b) under high intensity illumination and c) under saturated illumination.

3.1.2. Semiconductor / electrolyte junction

Differing from the semiconductor, the electrolyte is not an electronically conducting phase. Instead of electron-hole pairs, ions play the role of the charge carrier for the electrolyte, and the charge transfer is attributed to the redox reaction. A typical one-electron reaction can be written as:

$$O + e^- \rightarrow R$$

where O is oxidant, R is the product of this reduction reaction. This reaction is called half reaction, and O and R are defined as one redox couple. $E_{F,redox}$ of this given redox pair is determined in terms of the standard chemical potentials of O and R:

$$E_{F,redox} = \mu_R - \mu_O$$

The $E_{F,redox}$ therefore plays the same role as the E_F of a metal in contact with a semiconductor, which allows the construction of band diagrams. Electronic equilibrium can be achieved by an electron transfer across the semiconductor / electrolyte interface.

The standard electrode redox potential, U^0_{redox}, is defined as the potential difference (*i.e.* voltage) between a metal electrode in contact with the redox-contained electrolyte and a second metal electrode in contact with a solution containing protons (pH = 0) and hydrogen (in equilibrium with H_2 in the gas phase at a pressure of 1 bar). This second electrode is named after the standard hydrogen electrode (SHE) serving as the arbitrary potential zero.

The four most fundamental half reactions related to water splitting are listed in Table 1, and their corresponding electrical potentials (vs SHE) are also presented.

Table 1. Half-reactions and their corresponding standard electrode potentials concerning the water splitting.

Electrolyte	Photoelectrode redox pair	Half-reaction			Electrode Potential eV vs SHE
Acide pH=0	Anode H_2O/O_2	$2\ H_2O$	↔	$O_2\ (g) + 4\ H^+ + 4\ e^-$	E = 1.229
	Cathode H^+/H_2	$2\ H^+ + 2\ e^-$	↔	$H_2\ (g)$	E = 0.0
Base pH=14	Anode OH^-/O_2	$4\ OH^-$	↔	$O_2\ (g) + 2H_2O + 4\ e^-$	E = 0.4
	Cathode H_2O/H_2	$2\ H_2O + 2\ e^-$	↔	$H_2\ (g) + 2\ OH^-$	E = -0.828

It should be noted that the electrochemical potential of electrons (and hence E_F) in semiconductors is usually defined versus the vacuum energy level, whereas that of a redox pair is vs SHE as aforementioned. The redox Fermi energy of SHE, $E_{F,SHE}$, is commonly accepted as -4.5 eV.[78] We can convert from the SHE voltage scale to the vacuum scale based on the following equation under a standard situation:

$$E^0_{F,redox} = -4.5eV - qU^0_{redox}$$

Similar to semiconductors, the energy levels split into occupied (R) level and vacant (O) level for the charge difference between O and R. The electron energy distribution of the redox couple, W(E), is displayed in Figure 10 a, illustrating the probability of the fluctuation of the electronic energy level as a consequence of dynamic changes in the ionic environment.[79] The intersection point corresponds to the $E_{F,redox}$, where the probabilities of the redox electron level being occupied or unoccupied are equal. In the electrolyte electrons are localized on energy levels of ions, hence a change of the ion charge (*i.e.* an electron is added to the O level or removed from the R level) triggers an additional reorganization of the solvent around the ions (double layer or the Helmholtz layer) during the reaction. An adiabatic electron transfer happens only if the O and R energies are the same. In other word,

an adiabatic electron transfer is possible when the O and R states in the region where their W(E)s overlap.

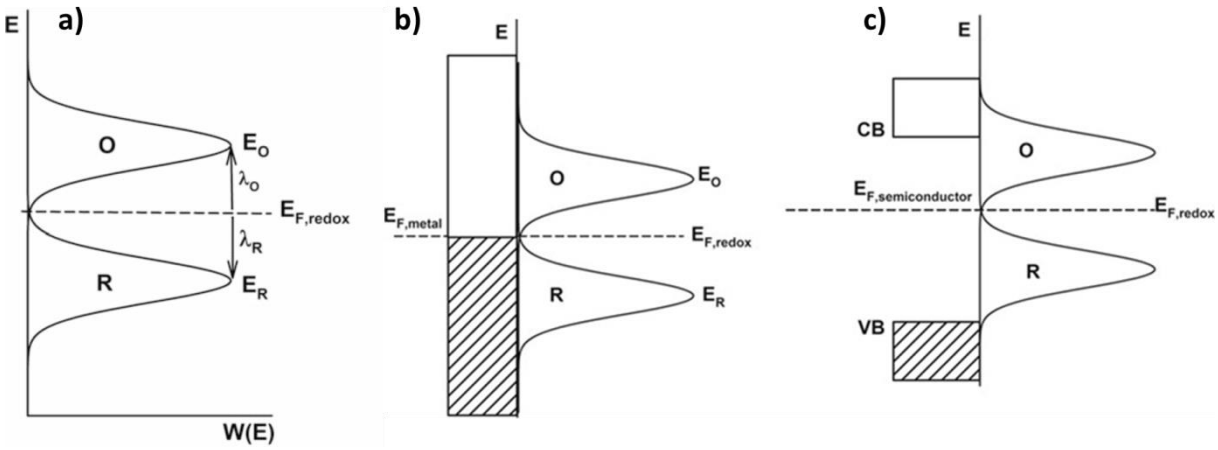

Figure 10. a) Gaussian probability distributions for a redox couple, assuming that the concentrations of O and R are equal; The intersection point is $E_{F,redox}$. b) and c) Comparison of the redox equilibrium at metal and semiconductor electrodes.[75]

The comparison of the band alignment between a metal / electrolyte junction and a semiconductor / electrolyte junction is shown in Figure 10 b and c. The E_F of metal indicates the boundary between occupied (slashed) and unoccupied energy levels (Figure 10 b), close to where the electron exchange will take place with the redox couple within the electrolyte. Because of the feature of semiconductors, the forbidden gap, only states above CB as well as those below VB, can overlap with the O and R states. Therefore, the reduction of O occurs through an electron transfer from CB or a hole injection into the VB. In contrast, R is oxidized with either an electron injection into CB or a hole transfer from the VB. It is the band offset between the semiconductor and electrolyte that decides the exact mechanism. Figure 11 displays several common semiconductor band positions comparing to the electrode potential of the two redox pairs (H^+ / H_2 and H_2O / O_2) at pH = 0.

When a semiconductor is initially immersed in an electrolyte under dark and non-bias conditions, an equilibration of the chemical potentials occurs if $E_{\mathrm{F,semiconductor}} \neq E_{\mathrm{F,redox}}$. We take the p-type semiconductor / electrolyte junction as an example. Supposing that $E_{F,redox}$ is more positive (vs vacuum state) than $E_{F,semiconductor}$, holes will spread out from the semiconductor surface and a space charge layer is formed. The band bending of semiconductors stops at the edge of its space charge layer. Since the majority carriers are depleted in the space charge area, this specific layer is also called “depletion region”. Once the equilibrium is reached, $\mathrm{E'_{F,semiconductor}} = \mathrm{E'_{F,redox}}$. Figure 12 a-d illustrate the distribution of charges, the electrical field, and the electrical potential across the semiconductor / electrolyte interface. The majority of the potential drop across the junction happens in the space charge region (SCR) as displayed in Figure 12 c. A built in voltage (V_{SC})

within the semiconductor is generated as marked in Figure 12 d. qV_{SC} is equal to the semiconductor Fermi energy difference between before and after contacted and equilibrated with the electrolyte. If the dopant concentration (N_D) and V_{SC} are known, the space charge layer width (W_{SC}) can be calculated based on the following equation:

$$W_{SC} = \sqrt{\frac{V_{SC}}{\frac{qN_D}{2\varepsilon_S}}}$$

where q is the standard electronic charge and ε_S is the static dielectric constant. It can also be deduced that $W \propto \sqrt{1/N_D}$.

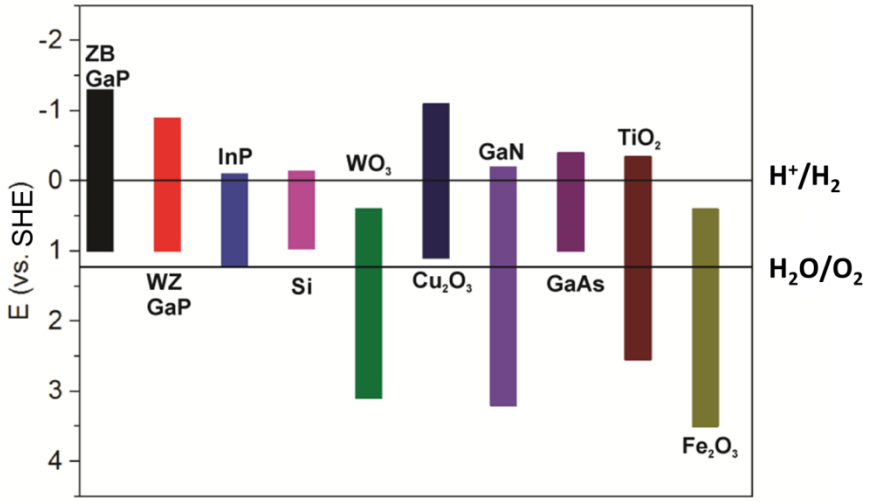

Figure 11. Band offsets between several semiconductors and the electrolyte (pH = 0), calculated from Mott-Schottky type measurements.[80]

The change in the semiconductor side has already been discussed. Now we discuss about the electrolyte side. The fixed space charge in the semiconductor balances with an opposite signed net charge in the electrolyte (Figure 12 a). The potential shift also occurs in the electrolyte close to the interface. Besides the potential drop at the depletion region V_{sc}, there are two more regions where the potential decrease can appear: one is the Helmholtz layer of the electrolyte where ions are quite close packed, the corresponding potential drop is termed as V_H; and the other is in the Gouy region where ions are relatively loosely arranged, the potential decrease is V_G. It should be noted that the SCR is generally much wider than the Helmholtz layer. The total potential drop V_t can be expressed as:

$$V_t = V_G + V_H + V_{sc}$$

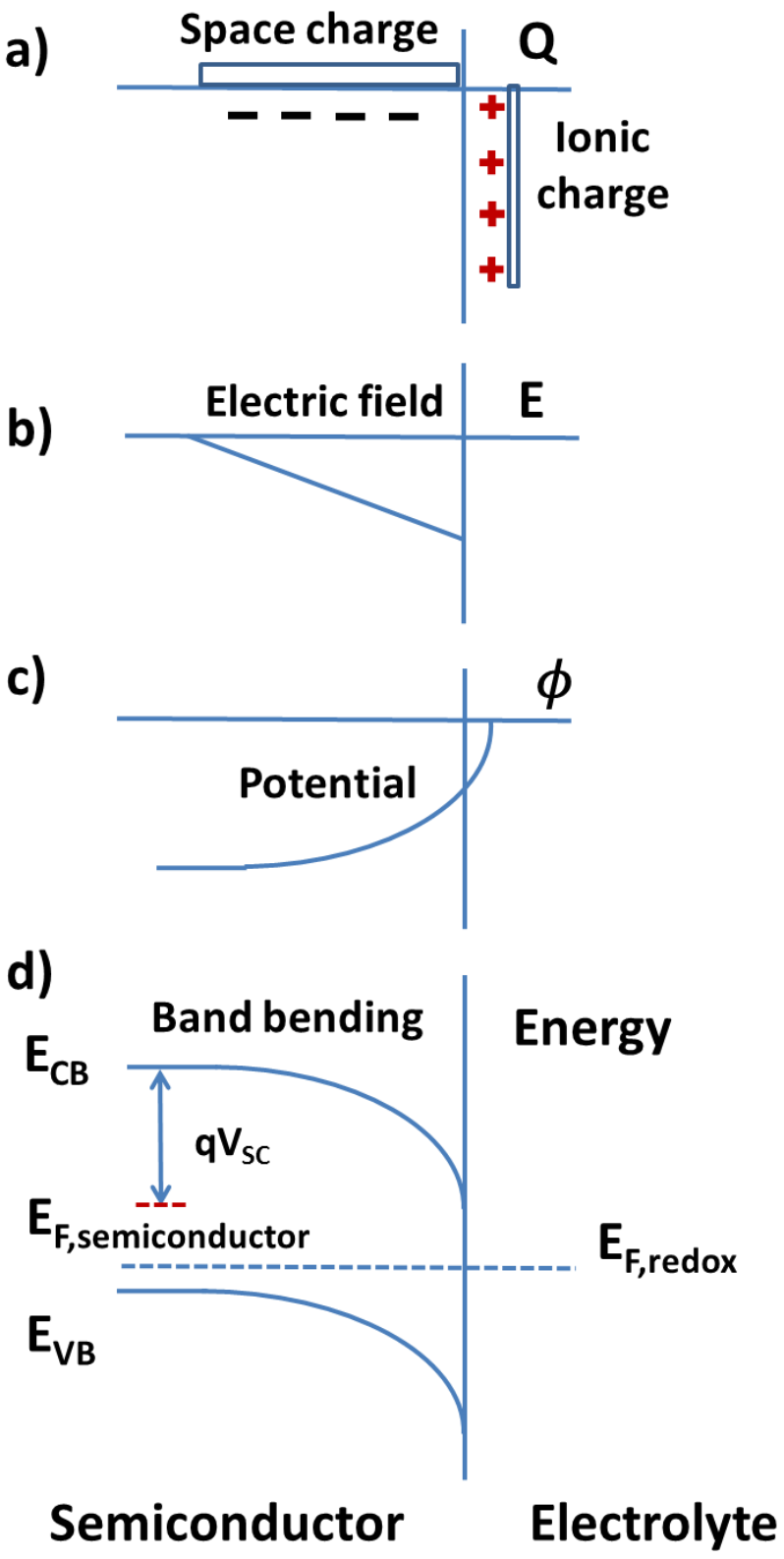

Figure 12. p-type semiconductor / electrolyte interface ($E_{F,redox}$ is more positive than $E_{F,semiconductor}$): a) charge distribution, b) electrical field gradient, c) electrical potential distribution, and d) band bending in the depletion layer.[75] The red dashed line in d) is the $E_{F,semiconductor}$ without contacting the electrolyte.

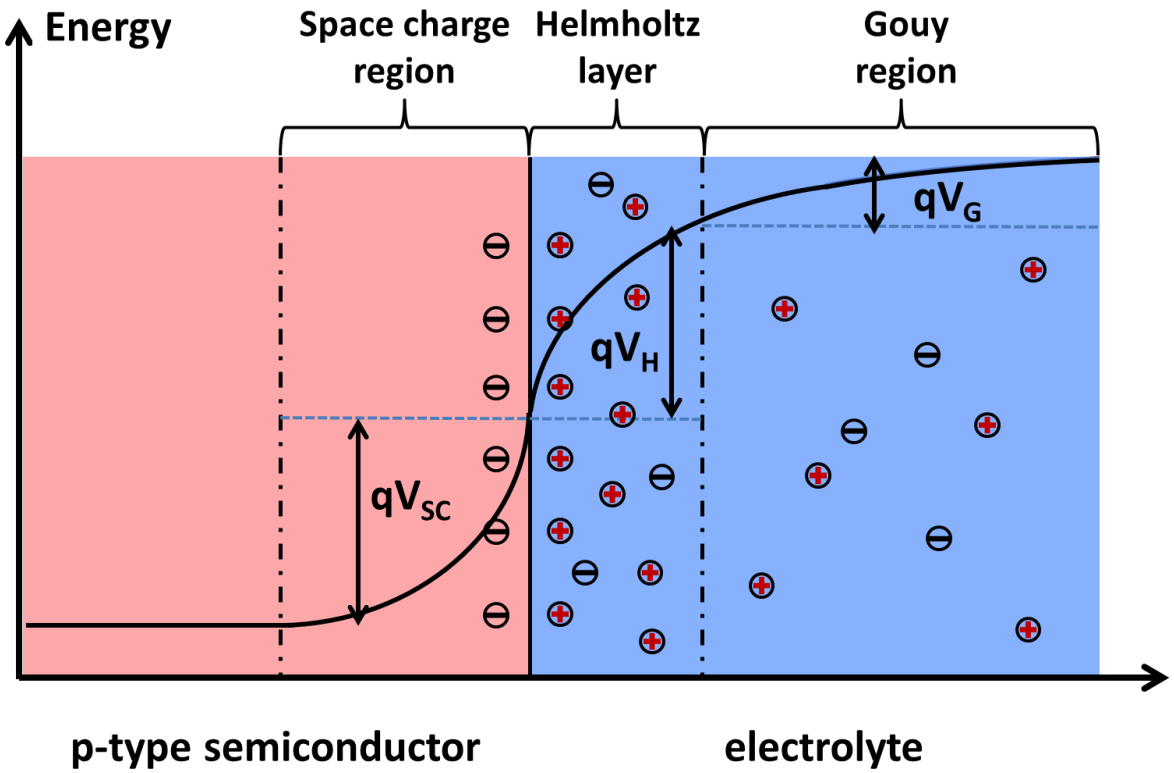

Figure 13. The electric potential drop within the p-type semiconductor / electrolyte junction under dark without bias.

Another important concept is the flat band potential. If $E_{F,redox}$ of the electrolyte is equal to $E_{F,semiconductor}$, there is no net charge transfer through the junction and hence no SCR. This is called the flat band conditions. This critical situation can be practically obtained by manipulating the electrode potential via an applying bias. The applied bias that just vanishes the SCR (the SCR width W_{SCR}=0) is the so-called flat band potential, U_{fb}.

3.1.3. Surface states and Fermi level pinning

Electron-hole pairs in semiconductors recombine via five processes as shown in Figure 14.[81] They can recombine via the radiative or non-radiative recombinations in the bulk of the semiconductor (bulk recombination, J_{br}), in the depletion region (J_{dr}), and at the surface containing defects (J_{ss}). The majority carriers can transfer to the O species in the electrolyte by thermally surmount the interfacial potential barrier (thermionic emission, J_{et}) as well as by a tunnel effect through the electric potential barrier near the surface (J_t).[77] Only the recombination concerning the surface states will be discussed below.

As aforementioned, it is also possible for semiconductors to store electronic charges due to the existence of surface states. Concerning a pristine solid surface in vacuum, intrinsic surface states are resulted from the symmetry-breaking discontinuity of the crystal lattice, while extrinsic surface states arise from either crystal defects or bonding with a solid or

liquid heterophase. The bonding interaction is due to the fact that the termination of the crystal lattice releases free bonds of surface atoms (dangling bonds) which can cause surface reconstructions by bonding with neighbouring atoms as well as with solvent molecules. Because of the change of the surface structure, the surface possesses energy levels different to the bulk.

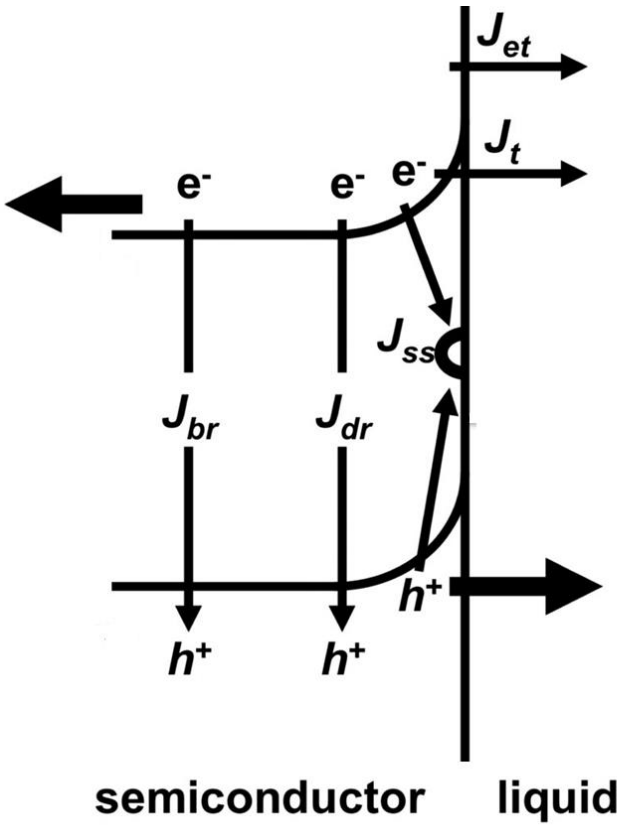

Figure 14. Recombination pathways for photoexcited carriers in a semiconductor / electrolyte junction at V_{oc}.[77]

These so-called surface energy states are usually located within the band gap and can affect the band bending within the SCR by accepting charge carriers. Moreover, surface states are generally deep levels, and quickly filled by the band bending causing minimal complications. Instead of the $E_{F,redox}$, the surface states can sometimes dictate the V_{SC}, which is referred to Fermi level pinning. It is the Fermi level that is pinned rather than the band edges. In practise, it is unfortunately very difficult to obtain ideal semiconductor / electrolyte junction without surface states. If the lifetime of bulk carriers is long enough, they can diffuse to the semiconductor surface and recombine at surface states. The surface recombination is an important loss mechanism in many devices. In the case of PECs, surface recombinations compete with interfacial electron transfers, lowering the quantum efficiency.

3.1.4. Semiconductor / electrolyte junction under bias

In a PEC cell, besides the illumination, the applied bias also influences the semiconductor / electrolyte junction behaviour. Still assuming that the $E_{F,redox}$ is more positive than $E_{F,semiconductor}$ for a given p-type semiconductor electrode. At open circuit without illumination, the equilibrium is reached as aforementioned. The corresponding band offset is shown in Figure 15 a.

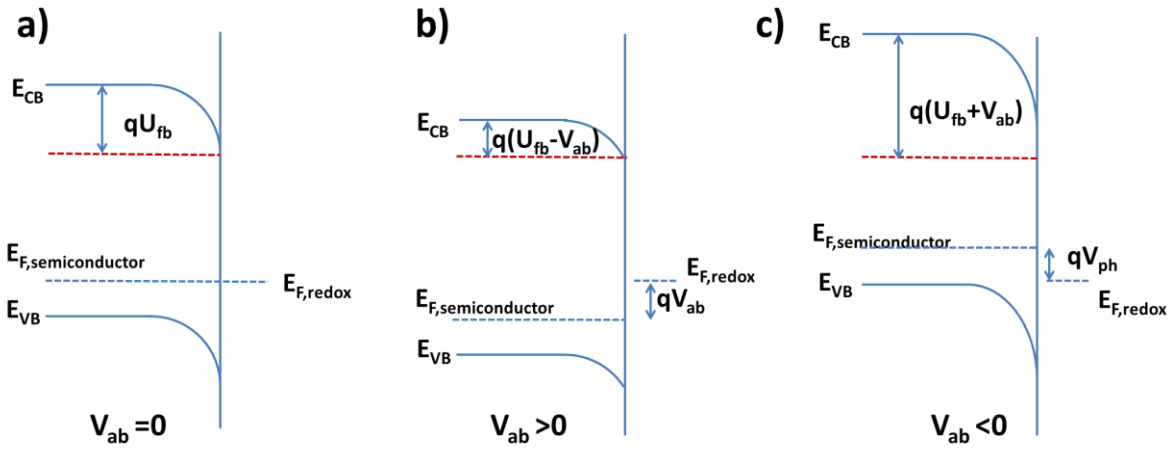

Figure 15. Band diagram of the p-type semiconductor / electrolyte junction in the dark: a) at the equilibrium situation, b) under positive bias, c) under negative bias.

The effect of an applied bias (V_{ab}) on the band bending is illustrated in Figure 15 b and c. When a positive bias is applied ($V_{ab} > 0$, Figure 15 b), the band bending is decreased and holes tend to accumulate at the semiconductor / electrolyte interface. On the contrary, $E_{F,semiconductor}$ shifts positively with respect to E_{redox} by applying a negative bias ($V_{ab} < 0$, Figure 15 c). This increases the semiconductor band bending, causing the electron accumulation at the semiconductor / electrolyte interface and intensifying the hole depletion. Hence a negative bias facilitates the separation of the photogenerated exitonic pairs and enhances the HER for the p-type semiconductor.

3.1.5. Overpotential and onset potential

The definition of overpotential is well-established in the electrochemistry field for describing the difference between the applied potential and the equilibrium potential in the case of metal electrodes. However, in the PEC field, the overpotential (η) is used to express the difference between the quasi Fermi level of minority carriers and the redox Fermi level. The onset potential (V_{on}) of a PEC cell is the critical applied potential at which the reaction begins apparently. V_{on} , V_{ph} and η obey the relationship as follow:[82]

$$V_{on} = E_{F,redox} - V_{ph} + \eta$$

3.1.6. Transient photocurrent

Transient variations of the photocurrent, shortened as transients, are related in part to bulk and surface recombination phenomena.[75,83] It is more visible by applying a chopped incident light. When the light shines on the photocathode, an excitonic pair is created and quickly separated by the applied bias. The electron reaches the semiconductor surface, where a competition between the water reduction (electron transfer from the cathode to the electrolyte) and the recombination in the space charge region and at the surface, occurs.[75] If the water reduction kinetic is too slow, electrons will accumulate at the interface, and the recombination process will be more predominant. If intra band gap states exist, the surface recombination can be further intensified. The surface charge dynamics related to transients due to chopped illumination are illustrated in Figure 16 as a function of the time at a given applied potential. The real photocurrent profile under illumination (left panel, corresponding to the part labelled "ON") includes four different regimes, displayed on the right panel of Figure 16:

Phase a: ideal behaviour, presenting a maximal photocurrent;

Phase b: because of the slow reaction kinetic, electrons accumulate at the semiconductor-electrolyte interface, some are gradually trapped at the semiconductor surface;

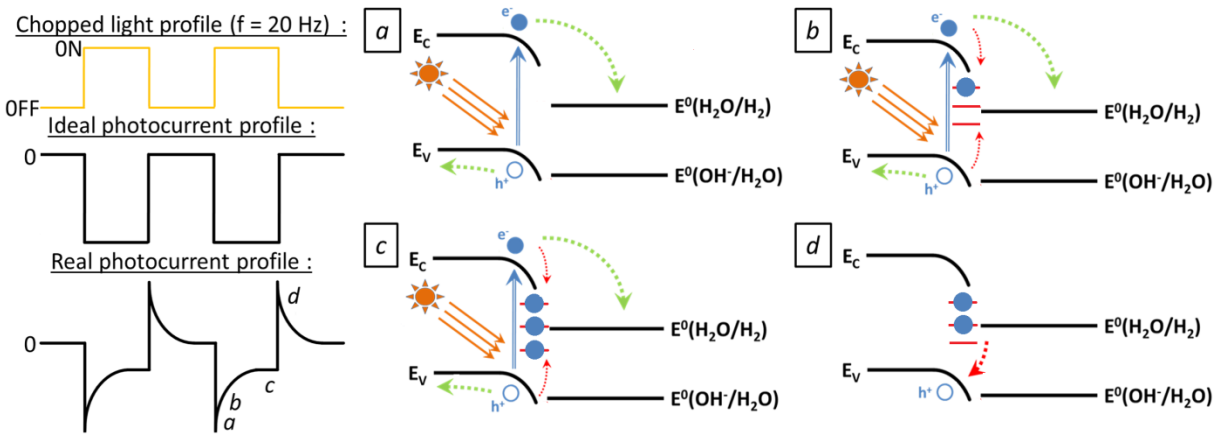

Figure 16. Chopped light induced transient phenomena. Left panel: chopped light profile and associated ideal and real photocurrent profiles. Right panel a-d): surface charge dynamics for the four different phases.

Phase c: photo-generated charge carriers that participate to the surface recombination balance with the ones involve into the water splitting reaction, the equilibrium state is reached, featuring a plateau, a steady current density;

Phase d: right after turning off the light, the holes move to the surface to recombine with the residual electrons, featuring as a transient current of opposite sign to the photocurrent.

The transients can be supressed by increasing the applied potential on the working electrode. In essential, higher potential can accelerate the water splitting kinetics.

3.2. III-V semiconductor NWs for water splitting

Since the pioneering work done by A. Fujishima and K. Honda, using a single-crystal n-TiO_2 as photoanode in 1972,[84] PEC water splitting has drawn the attention of the research community. For a rather long time, metal oxide semiconductors with a wide band gap (more than 2.3 eV) have been the most studied materials thanks to their efficient charge separation, low cost as well as photo- and chemical stability.[85] However, their wide gap feature makes them active only in the ultraviolet (UV) region, corresponding to less than 5% of the total energy of the solar spectrum.[86] Therefore, materials possessing a better absorption in visible region as well as in the infrared region are pursued. Even though efforts are put on to tailor the bandgap of metal oxides and enhance their charge carrier collection efficiency,[87,88] the status of narrow bandgap materials is growing.

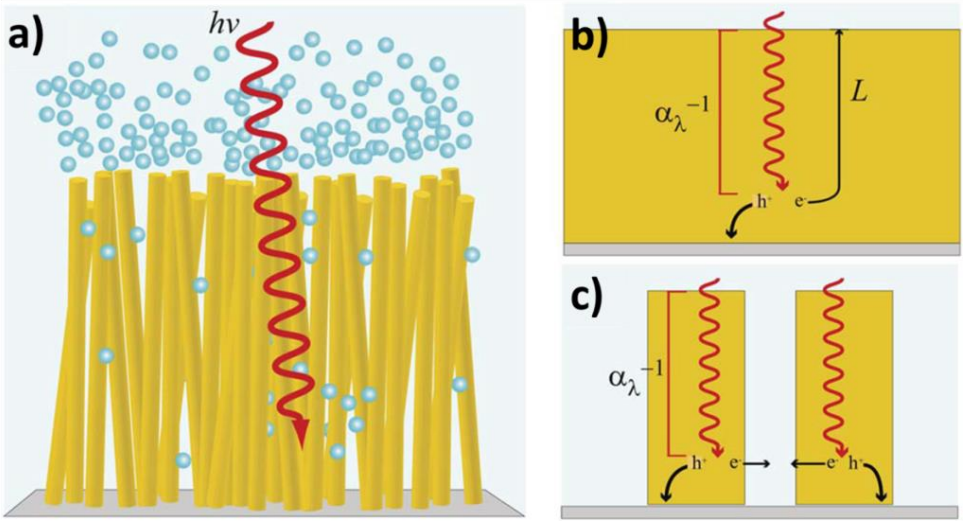

Figure 17. a) NW array working as a photoelectrode for PEC cell; Photogenerated charge carrier behaviour at b) planar and c) high aspect ratio NW photoelectrodes. The gray bottom represents the back contact for the majority carrier collection.[93]

Among narrow band gap semiconductors, Si (1.1 eV) is no doubt an extremely attractive candidate for its earth abundancy and well developed industry with a vast knowledge base.[89] But its indirect band gap and infrared light absorption can't meet the needs for efficient energy conversion. III-V semiconductors are another attractive materials. A lot of III-V semiconductors have suitable direct band gap as well as the appropriate band edge position.[80,90,91] Further, the band gap of III-V semiconductors can be easily tuned via a chemical composition control (synthesis of ternary even quaternary III-V semiconductors).[90] The corresponding light absorption can be achieved in the ultraviolet region, visible light region and even in the infrared region, thus covering the entire solar spectrum.[92]

The NWs themselves can decouple the light absorption direction and the minority carrier transport direction,[93] as shown in Figure 17. The charge separation and collection efficiencies can then be improved comparing to the planar films. Since the water splitting related reactions occur at the interface of semiconductor / electrolyte, NWs also provide a dramatically enlarged specific surface area, in turn active sites for the reaction increase. This also reduces the electrode overpotential, and diminishes the transient current (Figure 18 b).[94] The textured substrate shows less reflection and the light path is subsequently lengthened inside the device (Figure 18 a),[91] which is beneficial for the solar light absorption. Besides, the surface wettability can also be improved in a NW-based device, as shown in Figure 18 c-f. The contact angle of electrolyte on InP substrate is much bigger than that of the nanotextured one, and the photogenerated gas bubbles are efficiently released in the latter case.[95]

A NW array epitaxially grown on the crystalline substrate shows a wider spectral range for light emission and absorption than its planar film shaped counterpart, because strains induced by the lattice mismatch in heterostructures can elastically relax via the free NW lateral facets.[92] It is also feasible to exfoliate a NW array from the substrate and fabricate flexible devices while achieving the recycling of the substrate.[96] Besides, the Fermi level pins at the NW sidewalls resulting in a radial Stark effect, which is advantageous for solar energy conversion devices.[97] Finally, tandem cells with double or multiple band gaps are also viable in a NW geometry.[86,98,99]

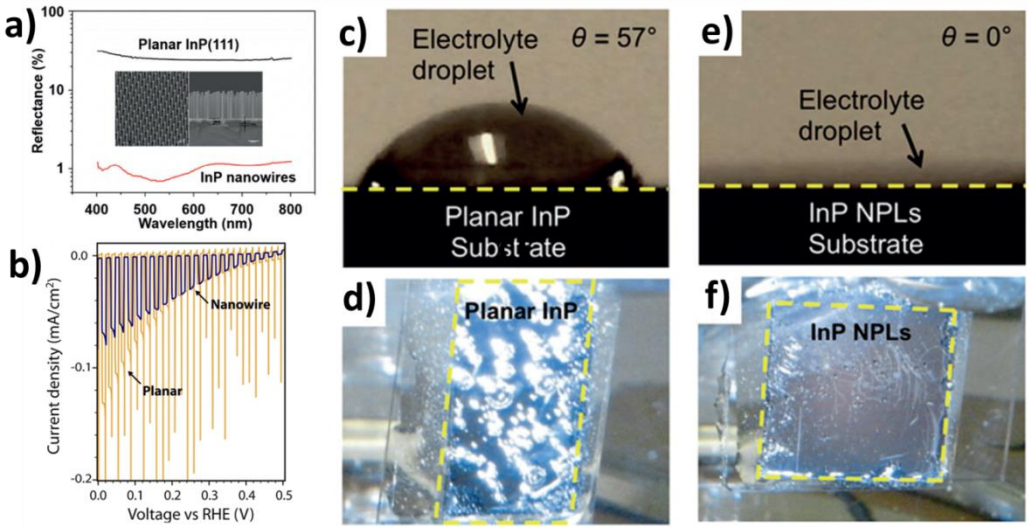

Figure 18. a) Reflectance for an InP NW array compared with a planar InP sample.[91] b) I-V curves of GaP NWs (blue) and planar (yellow) photocathodes under chopped illumination (AM 1.5 G).[94] c-f) Improved surface hydrophilicity for InP nanopillar photocathodes comparing to the planar InP substrate one.[95]

3.3. Semiconductor (core) / functional oxide (shell) NWs for water splitting

The large surface area of the NWs is expected to increase the surface recombinations as more surface states are introduced.[100] Passivation layers are studied for reducing the effect of surface states as well as protecting the NW photoelectrode from the corrosion.[80,101-103] Among all the passivation layers reported, metal oxides are the most promising conditates. Furthermore, titanium dioxide (TiO_2)[104-106] and aluminum oxide (Al_2O_3)[107,108] are the most well studied oxides. Figure 19 a illustrates the semiconductor Fermi level splitting when surface states are present. The passivation layer can basically work via two mechanisms: 1) the chemical passivation, 2) the field-effect passivation.[109] In Figure 19 b, a Si / Al_2O_3 NW heterostructure is used to show the chemical passivation against surface states, $E_{qF,n}$ doesn't pin at surface states and alignes with the $E_{F,redox}$. TiO_2 can also introduce an electric field at the surface which enhances the Fermi level splitting within the semiconductor (Figure 19 c). The large enough band gap of the TiO_2 (E_g = 3.2 eV) ensures the chemical passivation, and as the CB is positioned slightly above the reduction potential of water, the $E_{qF,e}$ aligns with the CB of TiO_2 rather than with $E_{F,redox}$, leading to a noticeable improvement of V_{OC}.[76] Besides the influence on the band alignment between the semiconductor and the electrolyte, the defects within the oxides could also serve as active sites increasing the absorption of water splitting related ions.[110]

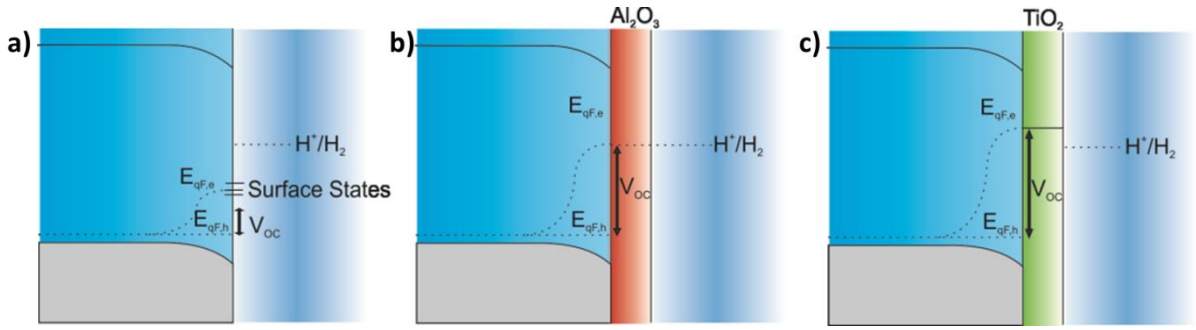

Figure 19. Schematic representations of quasi Fermi level splitting within the semiconductor a) in the presence of surface states, b) with Al_2O_3 passivation and c) with TiO_2 passivation.[76]

M. P. Warusawithana *et al.* and L. Ji *et al.* reported a Si-based photocathode with an epitaxial $SrTiO_3$ layer working as a photocathode for PEC cell.[111,112] Since the lattice mismatch between Si and $SrTiO_3$ is as small as -1.7%, crystalline $SrTiO_3$ can be grown on Si with a very low interface state density.[113] Photogenerated electrons can be transported easily through the $SrTiO_3$ / Si junction because of the high quality interface. Taking into the consideration of the structure similarity between Si and III-V semiconductors, $SrTiO_3$ might be applied into III-V NWs as a passivation layer for water splitting.

4. The aim and scope of this thesis

This PhD mainly focuses on the GaAs (core) / perovskite $SrTiO_3$ (shell) growth which is part of the project about combining the perovskite oxides with III-V NWs for multifunctional devices. The NWs we fabricated during this PhD was devoted to PEC cells thanks to the collaboration with CEA-Saclay. The GaAs NW morphology optimization and the facet surface protection are also included as they are the necessary step for realizing III-V semiconductor / oxide heterostructured NWs.

In the beginning of this work, the growth of GaAs NWs by self-catalyzed VLS mode in MBE was studied. The geometry and the structure of NWs were optimized by manipulating the growth parameters because of its notable effect on the performances of practical devices (PEC cell in our case). Then the surface oxidation of GaAs NWs was thoroughly investigated via various characterization methods, as well as its negative effect on the subsequent epitaxial shell growth. A reversible arsenic (As) capping / decapping procedure was used to protect the GaAs against the oxidation as well as the unintentional contamination. This procedure could be a general way for sample transfers and undoubtedly encourage the coupling between different materials in different reactors.

Then different kinds of GaAs-based core / shell NW arrays were fabricated. Epitaxial hybrid growth was preferred since it offers well organized interface. A partial epitaxial GaAs / $SrTiO_3$ core / shell NW array was achieved which could open a new way for the combination of the properties of III-V semiconductors and perovskite functional oxides in the NW technology and benefit to the research on multifunctional devices. GaAs / $SrTiO_3$ / $BaTiO_3$ multishell NWs, GaAs / amorphous-TiO_2 NWs were also fabricated and then studied.

Finally, we moved to the construction of the device for water splitting based on GaAs NWs, taking the advantages of its 1D geometry feature and narrow direct band gap. The GaAs / $SrTiO_3$ NW array was first used for the realization of PEC cells but the obtained results showed that the heterostructured NWs need to be optimized for this application. Thanks to the former experiences on the oxide growth on GaAs via MBE in our lab, GaAs / TiO_2 NWs were then fabricated and used for enhancing NW's photo- and chemical stability to improve the PEC efficiency.

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Chapter 2. Experimental techniques

1. Introduction

This chapter is dedicated to present the main experimental techniques which are used during the PhD study. They are classified into three different categories based on which practical step they involved in, first the growth of NWs, then the NW characterisation and the final physical property measurements. The basic theories of these techniques are introduced, as well as some common problems and conclusions. This brief interpretation can make the following chapters more comprehensible, and avoid the unnecessary repeat of one same topic.

2. Facility for the growth of NWs: molecular beam epitaxy

2.1. Molecular beam epitaxy

The word epitaxy, etymologically originated from the Greek. *Epi* means “above” and *taxis* means “an ordered manner”. The epitaxial growth is an ordered growth mode for turning the deposited material into a crystalline overlayer of one well-defined orientation with respect to the crystal structure of the substrate. To achieve this so-called epitaxial growth as well as to interpret the growth mechanism, molecular beam epitaxy (MBE) arose. Various kinds of materials have been successfully synthesised, ranging from semiconductors to metals and to insulating oxides. It was first applied to the growth of compound semiconductors, which is still the most common usage because of the high technological value of such materials to the electronics industry. And now, engineers still keep developing the apparatus to expand the range of the available element sources and then MBE’s scope of applications. Furthermore, because of the extreme clean growth environment as well as the precise control over composition in MBE, crystalline interfaces are almost atomically abrupt. Unique structures, such as quantum dots, quantum wells, superlattices *etc.*, are possible to be produced.

MBE, as the name suggests, uses localized beams of atoms or molecules under an UHV environment to provide a source of the constituents to the growing surface of a substrate. Generally speaking, modern MBE systems consist of several vacuum chambers, each with a suitable pumping system. Moreover, modern tools of surface analysis are also integrated to MBE providing a real time analysis of the growing surface and its environment.

Figure 20 shows a schematic top view of a typical MBE growth chamber. A thin, crystalline substrate wafer is mounted on a heater block and faces the effusion cells used to evaporate the constituent atoms or molecules. Mechanical shutters driven from outside the MBE

chamber are used to switch the beams on and off. The beams impinge on the substrate kept at a moderately elevated temperature. Arriving atoms, hence, possess sufficient thermal energy to migrate over the surface to lattice sites of lower incorporation energy. Because of the extensive use of liquid nitrogen cooling walls surrounding the effusion cells and the growth chamber, the background pressure in the system remains very low (typically 10^{-10}-10^{-11} Torr), and beams flow along a single pass through the chamber before condensing on the substrate. This preserves the purity of the growing materials and at the same time allows the integration of non-destructive analyse techniques, such as the reflection high energy electron diffraction (RHEED). The RHEED system provides a diffraction pattern on a phosphor-coated glass window that is indicative of the ordering of the growing surface. Thus, the surface crystal structure changes can be observed in real time when the physical and chemical environment changes, *e.g.* when the surface is exposed to the source beams, changing the beam intensity or the substrate temperature (T_s). To avoid concentration gradients and inhomogeneous morphologies, the wafer is kept rotating continuously throughout the growth.

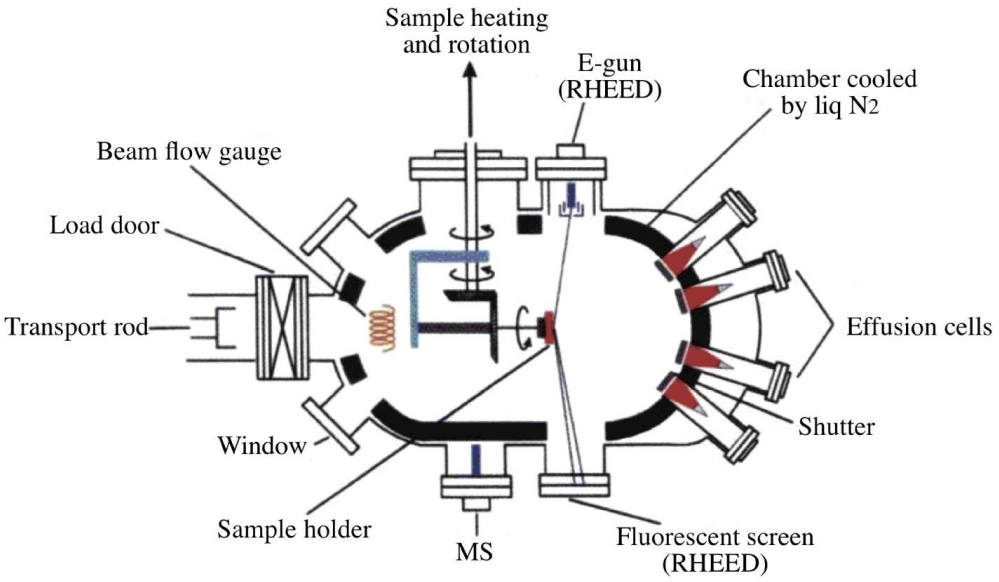

Figure 20. Top view of a MBE growth chamber.[1]

Measurement of T_s is surprisingly difficult. Since most semiconductor MBE systems are arranged to allow the substrate rotation during the growth process, directly bonding a thermocouple to either the substrate or the heater is not feasible. A non-contacting stationary thermocouple can be fixed behind the substrate to measure the radiant heat flux from the substrate, however only a relative substrate temperature is measurable. An accurate temperature calibration is further investigated via an infrared optical pyrometer within a range from 400 °C to 600 °C. If semiconducting substrates are used, the bandpass of the pyrometer must be chosen carefully; otherwise the pyrometer simply observes the

radiation from the substrate heater element that is transmitted by the substrate. It is also possible to know T_s based on the surface reconstructions observed on the *in-situ* RHEED pattern. For example, on GaAs substrates, T_S can be calibrated with the oxide desorption under arsenic (As) flux and the GaAs surface reconstruction which occurs at the temperature around 580 °C.[1] In our case, we have used an InP substrate for which the surface reconstruction changes from (2 x 4) to (2 x 1) at 470 °C (itself calibrated with respect to the fusion temperature of InSb under UHV at 525 °C) under a phosphorus pressure of $1x10^{-5}$ Torr.[2] This type of calibration can help us to know the real temperature for a Si substrate but it is not accurate enough. Hence we then chose to plot the temperature measured by the pyrometer T_{pyro} (the pyrometric measurements were performed through a glass window covered with a thin layer of III-V materials, assuming an emissivity of 0.4 at 1 µm) vs. the temperature measured by the thermocouple, T_{TC}, covering the entire temperature range of interest. The relationship between T_{pyro} and T_{TC} for one specific sample holder is presented in Figure 21. Instead of a constant temperature difference, it also reveals a gradually changing ΔT. The T_s discussed in the following chapters are all measured from the thermocouple.

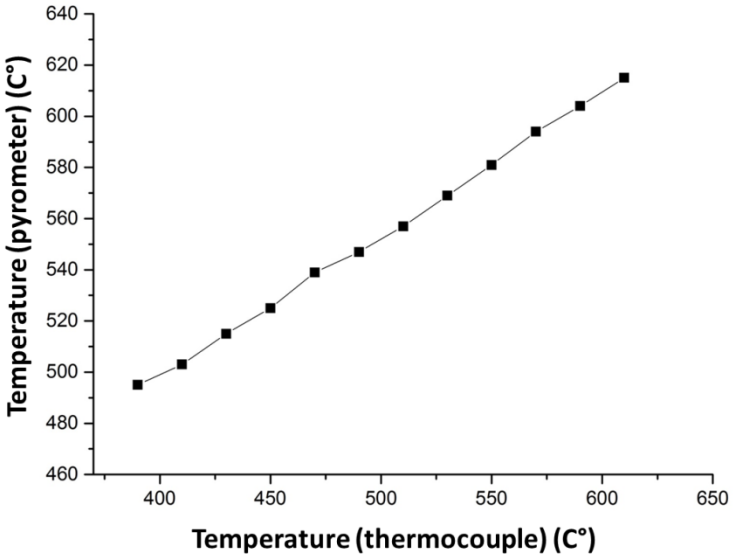

Figure 21. The relationship between the silicon substrate temperature measured by the pyrometer (with emissivity equal of 0.4) and the one measured by the thermocouple, for a specific sample holder.

2.2. Recipes for the NW growth

The MBE growth of NWs is achieved automatically via the software **EPISURE**. It provides a precise control of the shutter and the valve position, the programming of the temperature / heating power of the effusion cells and substrate, as well as the rotation speed of the sample. Herein, we present typical recipes for GaAs NW growth (Table 2). It should be noted

that the flux of Ga and As is kept identical every time, while the cell temperature of Ga and the opening of As valve can vary time to time. Recipes of radial GaAs NW growth, GaAs / $SrTiO_3$ core / shell NW growth and the GaAs / amorphous-TiO_2 core / shell NW growth are displayed in Appendix 2.

Table 2. Typical recipe of a GaAs NW axial growth on a Si(111) substrate.

Step	Time duration	Main shutter	Ga (°C)	Ga shutter	As valve (%)	As shutter	Substrate temperature (°C)	Ramp of substrate temperature (°C/min)
preparation	1 s	off	928	off	0	off	100	
temperature increase	10 min	on					450	35
Ga-catalyst deposition	2 s			on				
temperature increase	10 min		942	off			570	12
As_4 preparation	10 s	off			12	on		
GaAs NW growth	20 min	on		on				
cooling	10 min		928	off			100	without ramp
termination	10 s	off			0	off		

2.3. Reflection high energy electron diffraction (RHEED)

Taking advantage of the UHV working conditions, a lot of characterisation methods can be integrated to the MBE system. As far as the *in-situ* one, the RHEED system is undoubtedly the single most important and widely used analytical tool due to the specific geometry that there is no part of the RHEED system positioned in front of the sample to block access to the surface. Meanwhile, it is relatively insensitive to the ambient in the growth chamber, which means that RHEED images can be obtained with equal clarity either while beams are incident on the substrate or when the growth is terminated and the substrate is cooled.

The RHEED diffraction is very surface-sensitive, sampling merely very few atomic layers beneath the surface. The grazing incidence angle determines the penetration into the material. For a material with a smooth surface, in the construction of the reciprocal lattice we can therefore approximate the sampled volume as a 2D thin layer. The reciprocal lattice then degenerates into a set of 1D rods along the z direction perpendicular to the surface[3] and intersecting with the Ewald sphere (Figure 22) to form points which should be observed

on the RHEED screen. In fact, as the radius of the Ewald sphere is very large for an electron beam, the intersection of the Ewald sphere with the rods are not points but segments and these segments are observed as lines on the RHEED screen. For a material with a rough surface or for 1D and 0D materials, the diffraction is obtained by transmission through the roughness or through the 1D and 0D materials and the reciprocal lattice is formed of points. The intersection of Ewald sphere with the network of points is also a network of points which are observed as spots on the RHEED screen. The lines and spots (or rings for a polycrystalline material) on the RHEED pattern are indexed in a way similar to that used for the bulk diffraction.

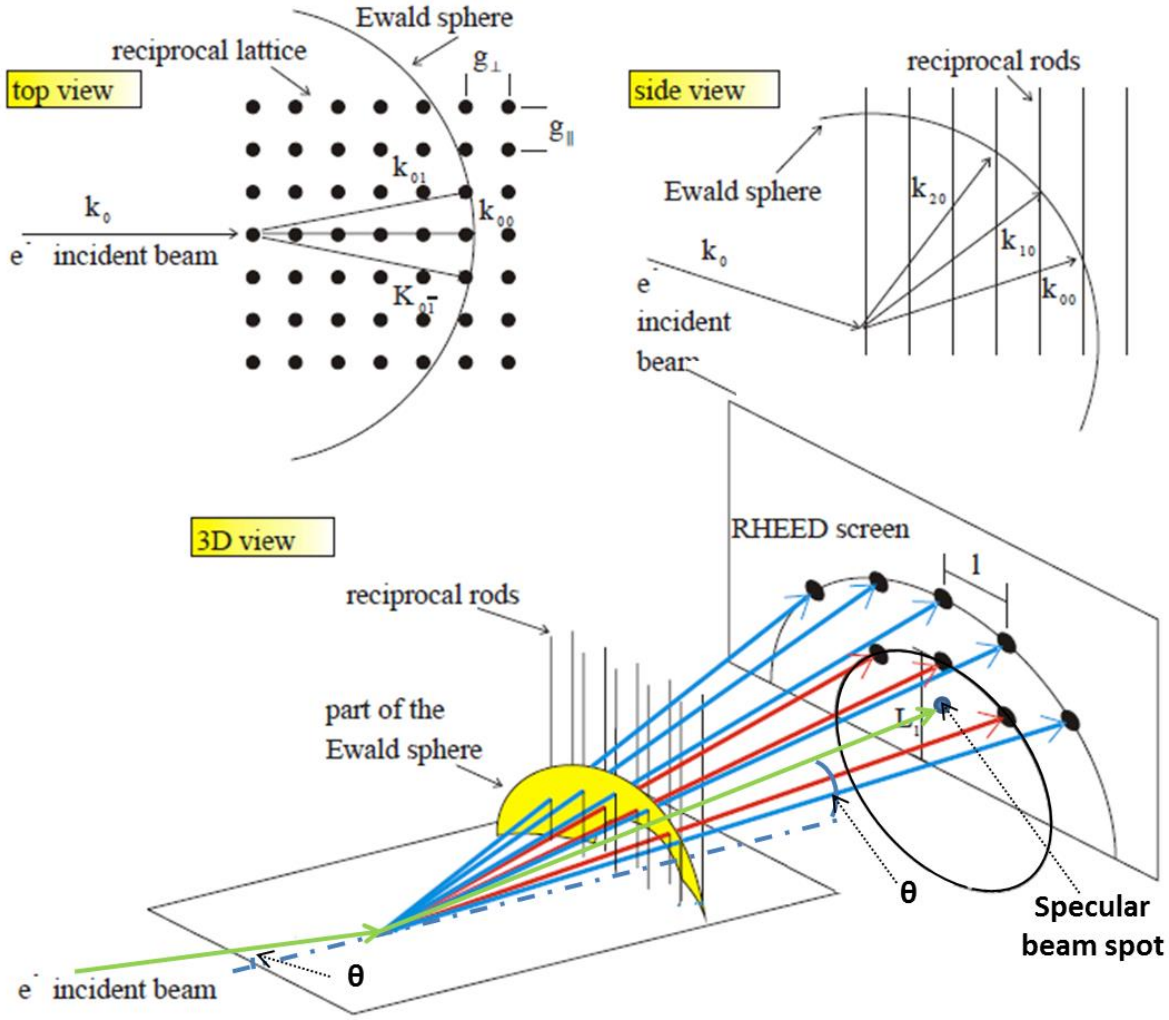

Figure 22. Ewald construction and diffraction geometry of RHEED.[4]

The RHEED has several important functions when adapted to MBE systems. First, the RHEED pattern gives useful information about the structure of the surface, including the roughness. Here, we present, as an example, the typical RHEED patterns of the as-grown GaAs NWs on Si(111) in two different azimuths, namely [1-10] and [11-2] (Figure 23 d, e). Based on the specific geometry of the RHEED diffraction, the pattern corresponds mainly to

the upper-most part of NWs. As known, self-catalyzed GaAs NWs prefer the cubic Zinc Blende (ZB) structure with an ABC stacking sequence (Figure 23 a), while hexagonal Wurtzite (WZ) structure (Figure 23 b) insertions are often detected. On the RHEED pattern taken from the azimuth [1-10], the two different structures, ZB and WZ, as well as the twin defects, can be detected. The most intensive diffraction spots are indexed in Figure 23 d and e. Diffraction spots unindexed in d) are attributed to WZ insertions in ZB GaAs NWs as well as to the parasitic GaAs crystals. The indexation of this type of diffraction pattern is detailed in Chapter 3. The RHEED system can also monitor the growth in real time, for a qualitative measure of the NW topography and structure. RHEED oscillations, first observed in the growth of GaAs layers by MBE,[5] are also used to measure 2D layer growth rates and to determine alloy compositions.[3]

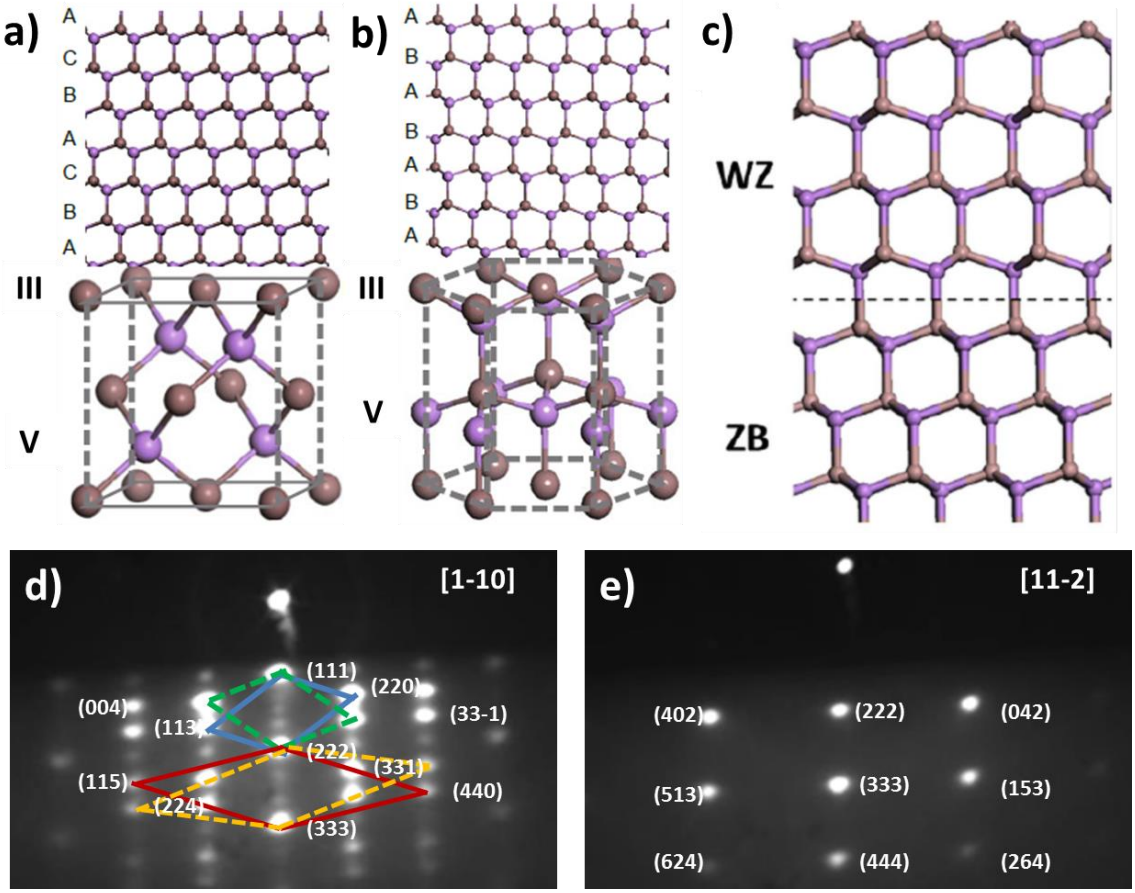

Figure 23. a) The ABC stacking and the unit cell for the ZB structure of III-V semiconductors, b) the AB stacking and the unit cell for the WZ structure of III-V semiconductors,[6] c) the interface between the ZB and WZ structures[7]. RHEED patterns obtained for self-catalyzed GaAs NWs on Si(111) along: d) [1-10] and e) [11-2] azimuths with the spot indexation. The characteristic [1-10] pattern of ZB GaAs with twin defects (marked by blue and green and by red and orange parallelograms) is observed. Spots unindexed in d) are attributed to the WZ insertion in ZB GaAs NWs as well as to the parasitic GaAs crystals. The indexation of WZ diffraction spots is detailed in Chapter 3. The RHEED electron energy is 30 keV.

All growth rates mentioned in this thesis are in terms of the equivalent 2D growth rate determined by measuring the RHEED oscillations during the GaAs layer growth on a GaAs substrate. The principle of the measurement is illustrated in the Figure 24. In the initial state, the layer surface is plane (θ = 0), so the specular beam is diffused in one same direction. The specular beam spot (sbs) intensity is thus the strongest. When a new layer begins to form, the electrons are diffused and the sbs intensity decreases (θ = 0.25). The minimum intensity is reached when the layer is half filled (θ = 0.5). The growth continues, the sbs intensity recovers gradually (θ = 0.75). And the maximum is regained when the layer is fulfilled (θ = 1). The intensity of the sbs oscillates between the maximum and the minimum values. The duration between two successive extrema can be used to determine the growth rate of one monolayer per second (ML/s).

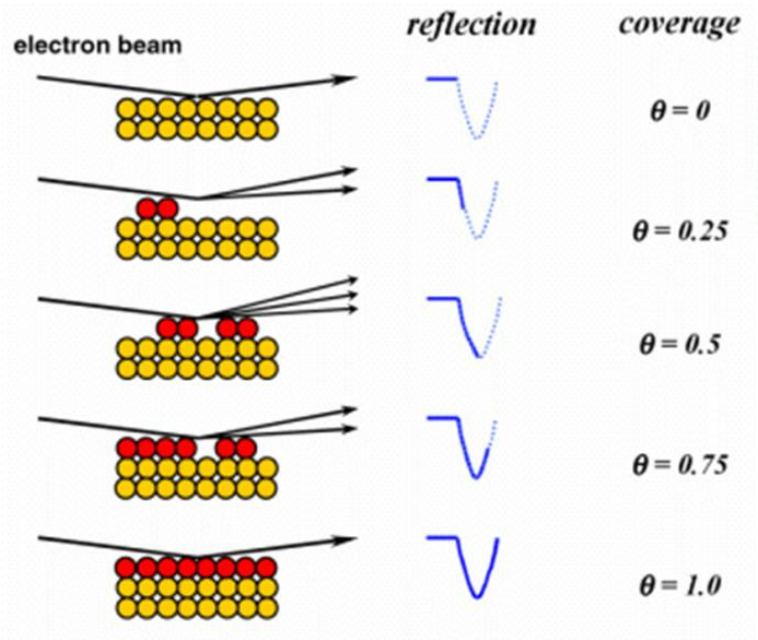

Figure 24. Elastic scattering model of RHEED intensity oscillation in 2D epitaxial growth (© Graduate School of Engineering, Tohoku University).

Use the growth of GaAs as an example. In most of the cases, the growth rate of GaAs is limited by the Ga flux when the growth takes place with an excess of the As pressure P_{As}

measured by the Bayard-Alpert gauge (or As beam equivalent pressure, As BEP). The Ga flux can be expressed in Å/s corresponding to the growth rate of the GaAs 2D layer measured by RHEED oscillations. In the same way, as proposed by D. Rudolph *et al.*,[8] the As flux can be also expressed in Å/s corresponding to the growth rate of the GaAs 2D layer when it is limited by the As flux. Our measurements were done under the As flux-limited condition, which means that P_{As} was fixed while the Ga flux was increased to get a corresponding saturation 2D layer growth rate. Figure 25 a shows Ga-As flux measurements obtained by monitoring RHEED oscillations. Each P_{As} corresponds a saturated GaAs 2D layer growth rate (in Å/s). It is then possible to deduce the relationship between the As flux (F_{As}) (Å/s) and P_{As} (Figure 25 b).

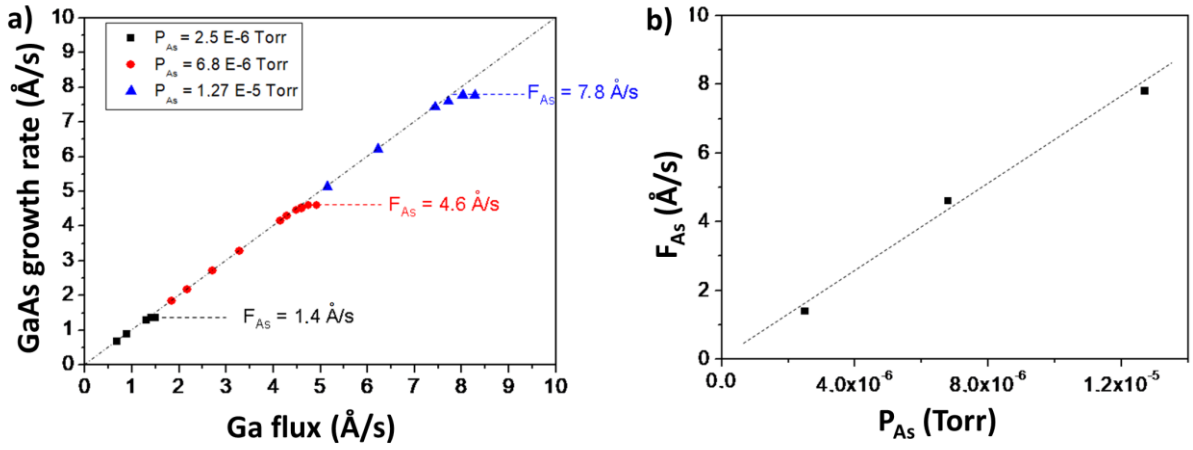

Figure 25. a) Ga-As flux measurements obtained by monitoring RHEED oscillations; b) F_{As} as a function of P_{As}.

In conclusion, MBE is a competent research technique for constructing epitaxial structures, attributing the unique combination of i) UHV conditions, ii) precise molecular beam flux control and iii) the integration of *in-situ* surface analysis tools. In the future, MBE should continue as an important research technique for material preparations. Doubtlessly, there will be an ever-stronger marriage of the MBE technique with more sophisticated analysis tools, for instance transmission electron microscopy, x-ray diffractometer, etc.

3. Facility for the characterization of NWs

3.1. Transmission electron microscopy

Transmission electron microscopy (TEM) is a microscopy technique in which a beam of electrons is transmitted through a specimen to form an image due to diffraction or mass-thickness contrast. A TEM consists of several components, including an electron emission source for the electron beam generation, a vacuum system in which the electrons travel in a series of electromagnetic lenses and electrostatic plates to guide and manipulate the beam

as required. Also an image system and a specimen related device allowing the sample insertion / withdraw, rotation, heating, *etc.* are also indispensable parts.

3.1.1. TEM imaging and electron diffraction

The wavelength of the light for illuminating the sample ultimately determines the available maximum resolution. Because there is a bottleneck using light as a way of magnification, the electron microscopy was born. For example, a 200 kV electron beam, results in an extremely small wavelength, ≈ 2.5 pm, much smaller than the wavelength of visible light (400 - 700 nm). This electron beam can reach a theoretical resolution even smaller than atoms themselves. The principle of TEM imaging, as well as the high resolution TEM (HRTEM), is shown in Figure 26.

Comparing to the general morphological analysis, the modern TEM offers as well a crystal structural measurement known as selected area electron diffraction (SAED) by adding a specific aperture in the image plane of the objective lens (Figure 26). This aperture filters all those electrons hitting outside the diaphragm of the aperture, in other words stops them to contribute to the diffraction. Hence, the as-generated electron beam are scattered in a limited volume of the specimen defined by the aperture size. The SAED patterns are displayed on the viewing screen at a magnification given by the camera length. This distance corresponds to the distance of the recording film or CCD camera from the diffraction plane of the objective lens.

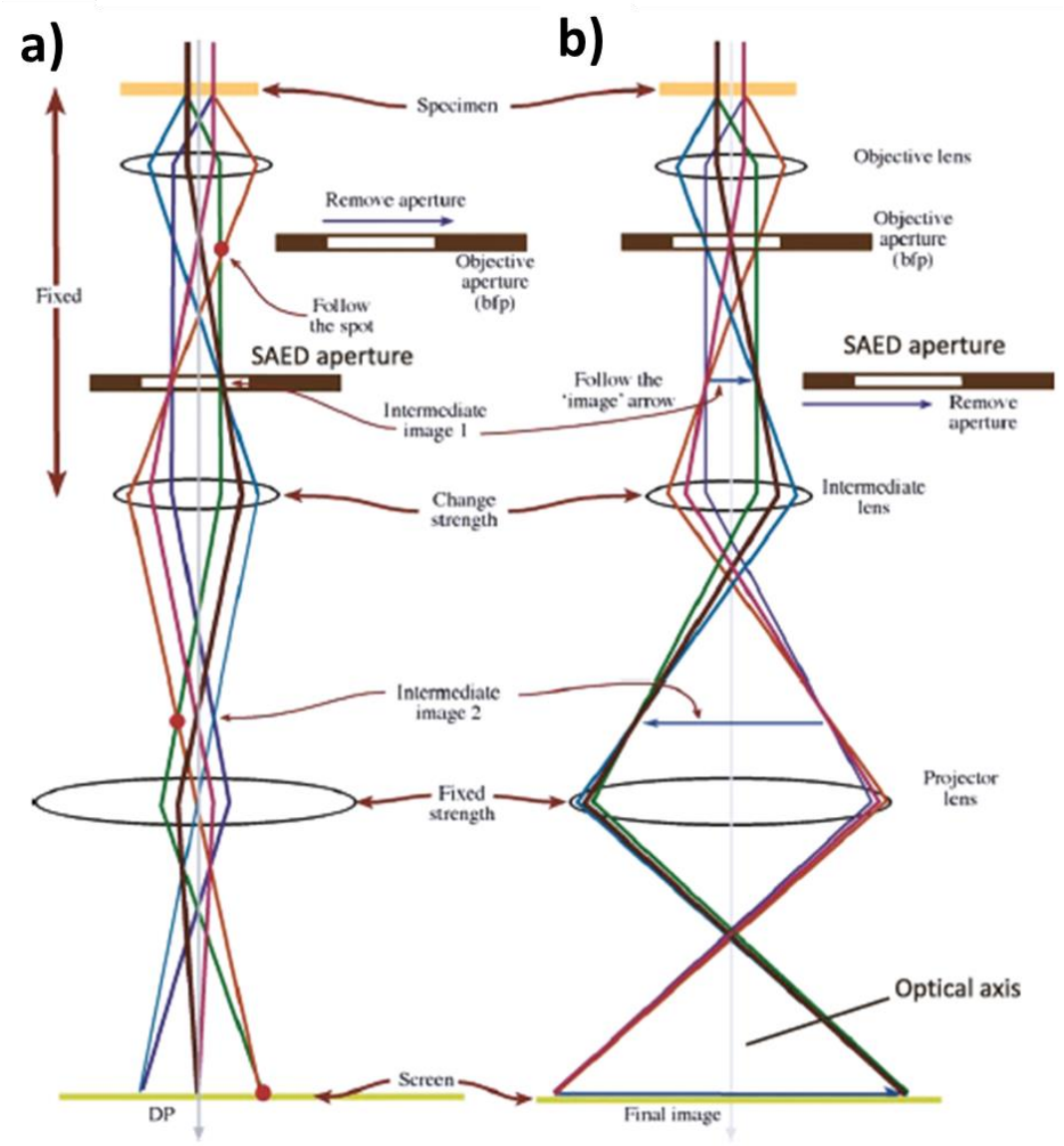

Figure 26. A schematic illustration of different electron beams along with lenses and apertures in the TEM microscope to perform a) electron pattern and b) imaging. In both cases, the sample is inserted into the UHV column where a parallel electron beam is incident on the sample. After passing through the sample, the electron beam splits into several beams due to Coulomb interaction and are guided through the lenses and apertures before imaging on the screen.[9]

3.1.2. Electron energy dispersive X-ray spectroscopy

TEM is quite often equipped with an electron energy dispersive X-ray spectrometer, shorted as EDX, allowing an elemental analysis. Because of the interaction between the electron beam and the atom within the sample, electrons in an inner shell of an atom is excited and ejected, leaving a hole in the inner shell. Then another electron drops from the higher-level shell of the atom to neutralize the hole while release a photon of a specific energy. The energy of this photon is equal to the energy difference between the two shells which is generally in the X-ray range. The energy and relative intensities of these X-rays can

be measured to provide an idea of the elemental composition of one sample. The EDX line scan and mapping can further give the elemental distribution information. It is worth noting that one element can emit several different characteristic X-rays: as the number of electron shells increases, more electron transitions can occur. For instance, an atom with K, L and M shells can have three types of X-ray: K (L to K), K (M to K) and L (M to L).

3.1.3. Sample preparation

The specimen for TEM is most often an ultrathin section less than 100 nm thick or a suspension on a grid. The most straightforward way to prepare NW sample is to disperse the NWs on a holey carbon grid. Basically, there are two ways for implementing the dispersion. The first method is to disperse the NWs in a relatively inert and highly volatile solution. A drop of the NW suspension is then put onto the TEM grid. The sample is ready after the complete evaporation of the solution. The other way is to place the grid directly on the substrate with NWs and move it around and scratch gently. The later works well, if the NW density on the substrate is high enough and the NWs are not too short (longer than 300 nm). In this work, we preferred the second method for its simplicity and without contamination introduced by the solvent. However, the operation should be as gentle as possible to avoid the deformation or the damage of the vulnerable grid.

3.2. X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) uses soft X-rays to excite core and valence electrons within the atoms of a surface. Photoelectrons are emitted from the material and their kinetic energies (KE) are measured by the instrument. Figure 27 illustrates this excitation process. The electron binding energy (BE) of each of the emitted electrons can be determined via the following equation:

$$KE = h\nu - BE - \phi_{spectrometer}$$

where $h\nu$ is the incident photon energy (h is the Planck constant and ν is the frequency of the photons) and $\phi_{spectrometer}$ is the analyzer work function (the minimum energy required for an electron to penetrate into the analyzer). A given photoelectron of one particular element corresponds a particular electron BE value. It is thus possible to index each XPS peak based on the BE. Due to the photoelectron ejection, holes remain in the sample surface. If the sample consists of a less-conductive material, the accumulated holes will cause a positive charge effect which decelerates the leaving photoelectrons (*i.e.* reduces their KE). The XPS spectrum displaces a shift towards higher BE side. To eliminate this charge effect, one can either use an electron gun to neutralize these photoemission-caused charges or determine the energy shift with the help of a referential photoemission peak. In this work, we generally used the C 1s peak at 284.6 eV as the reference.

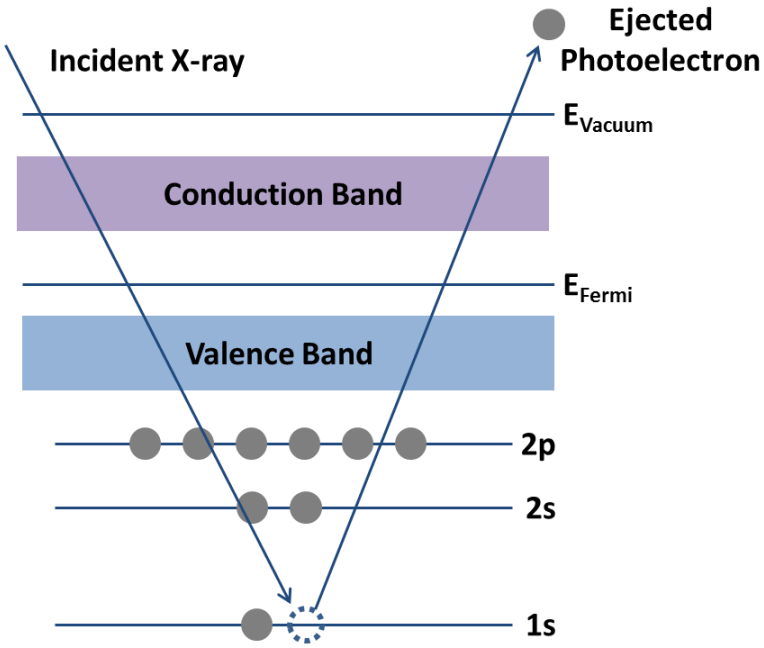

Figure 27. The photoemission process involved in XPS surface analysis.

Before detected, the photoelectron must first escape from the sample surface without interacting with overlaying atoms which leads to a loss of KE (inelastic scattering). The escaping probability of a photoelectron can be approximated through the Beer-Lambert Law:

$$I_d = I_0 e^{-d/\lambda}$$

where I_d is the photoelectron intensity originating from atoms at a given depth d, I_0 is the signal emanating from the surface atoms, and λ is the electron inelastic mean free path (IMFP). The IMFP represents the average distance that a photoelectron can travel before undergoing inelastic scattering and is dependent on the electron KE as well as the material properties.

Figure 28 display a schematic of an XPS instrument. The main components include a source of X-rays, an UHV stainless steel chamber with UHV pumps, an electron collection lens, an electron energy analyzer, a magnetic field shielding and an electron detector system. In our case, the XPS chamber is directly connected to the MBE chamber under UHV, possible for the *in-situ* measurements. Contrary to the RHEED, classical XPS does not give structural information, which makes the two techniques complementary as *in-situ* characterizations during and after the growth for structural and chemical analyzes of a sample.

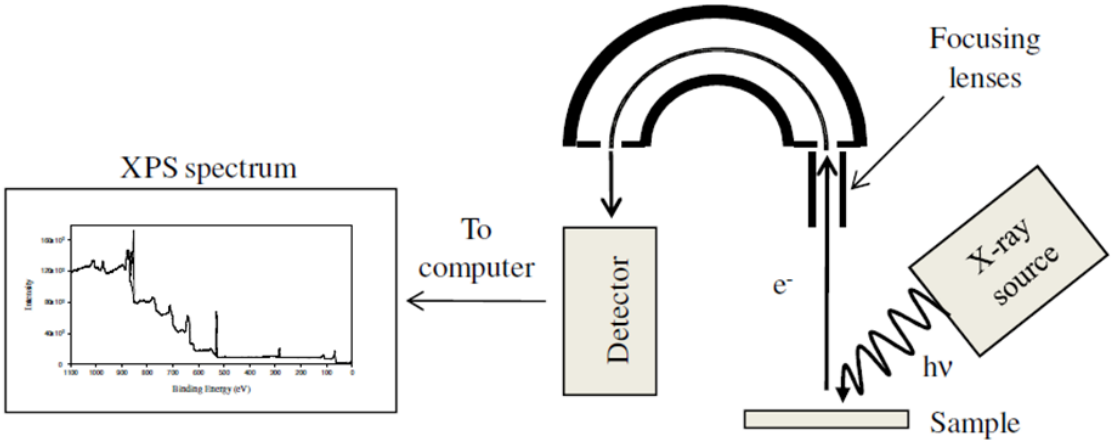

Figure 28. Simplified schematic of an XPS instrument.[10]

XPS measurements in this work were performed using a focused monochromated X-ray source (Al Kα = 1486.6 eV). Two types of spectra were obtained as follow:

- A general scan: a rapid scanning in a large range of BE to determine the BE windows for each relevant photoemission peak;
- High resolution specific spectra of core levels of different element within the sample material, acquired with good statistics.

All the raw data were background corrected using the Shirley method and then normalized. The fitting was achieved with Fityk 0.9.8.[11] The main fitting parameters used in this work are listed in Table 3.

Table 3. Fitting parameters used for the main XPS peaks in this work.

Core level	Binding energy (eV)	Spin orbit splitting (eV)
Ga $3d_{5/2}$ (GaAs)	19.1	0.45
As $3d_{5/2}$ (GaAs)	41.0	0.69
Ti $2p_{3/2}$ (TiO_2)	459.0	5.73
Ti $2p_{3/2}$ ($SrTiO_3$)	458.59	5.73
Sr $3d_{5/2}$ ($SrTiO_3$)	133.24	1.74
Sr $3d_{5/2}$ ($SrTiO_3$ stacking faults)	133.84	1.74

Sr $3d_{5/2}$ (SrO)	134.49	1.74

4. Facilities for the characterization of the NWs-based photoelectrochemical cell

Because of the 1D nanometric morphology, semiconductor NW array is very suitable for solar water splitting devices. The performance of our GaAs NW array was measured at CEA-Saclay (collaboration with H. Magnan) by constructing a photoelectrochemical (PEC) cell. The major feature distinguishes a PEC cell from a (dark) electrochemical cell is that one or both of the electrodes is photoactive, and thus needs light to drive the chemical reactions related to the water splitting. The water reduction happens on the surface of the photocathode manifesting a negative current, in other words, electrons are transferred from the working electrode to the electrolyte and finally to the counter electrode. On the contrary, the water oxidation occurs on the surface of the photoanode showing a positive current. Since solar water splitting is in essence a redox reaction using light-generated charges within the photoactive electrodes, the current measured by PEC characterizations is directly linked to the solar water splitting efficiency: the higher the current (absolute value) is, the more the evolved gas is produced.

The experimental setup is illustrated in Figure 29, the main components are listed as follow:

- An illumination source (Newport 1000 W Xe Arc Lamp);
- One manual and one automatic optical chopper (model 71445 from Newport and MC-2000 from Thorlabs respectively);
- A monochromator (Cornerstone model 74004 from Newport);
- A three-electrodes PEC cell (custom-made by Veral);
- A potentiostat (Princeton Applied Research 263A);
- A lock-in amplifier (PAR 5210);
- A power meter (model 1918-R from Newport) used for the light flux calibration (not shown);
- A computer to collect data and control the instruments (not shown).

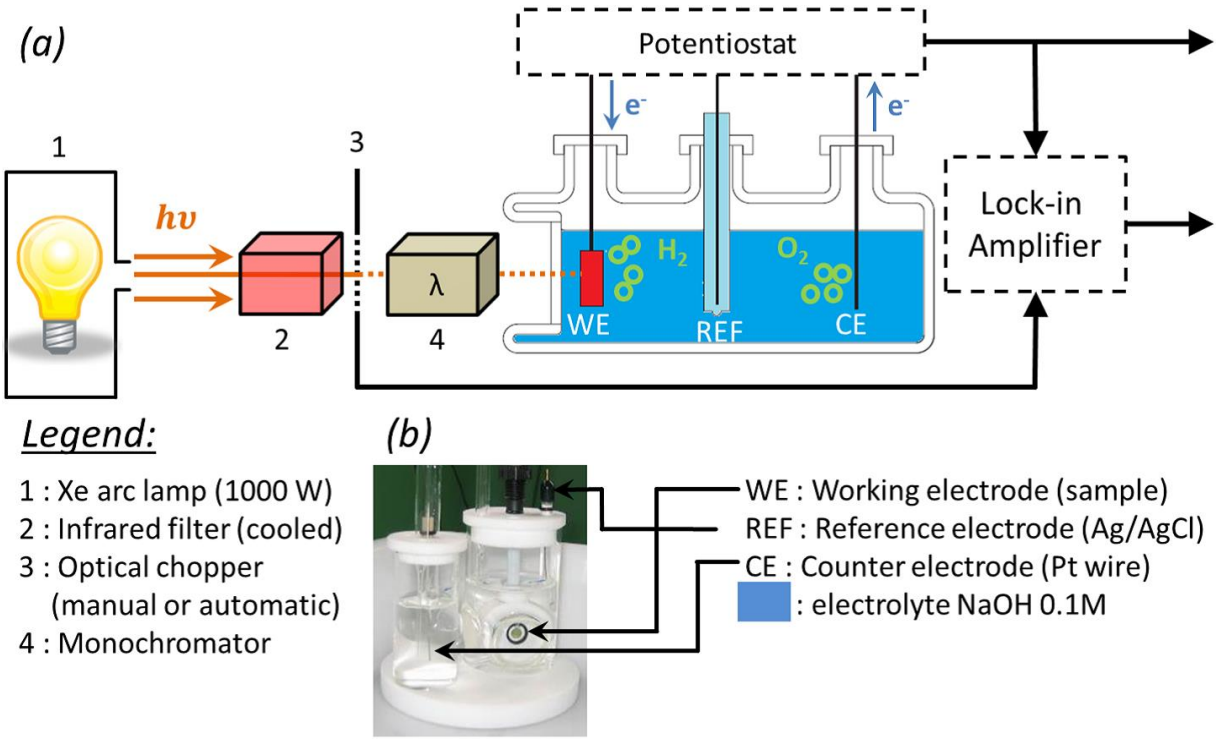

Figure 29. a) PEC setup, and b) details of the mounting within the PEC cell.[12]

4.1. The illumination source

The illumination source provides a light flux imitating the solar spectrum. In our case, an ozone-free Xe arc lamp is used as the illumination source. The lamp outgoing flux is calibrated by the monochromator and the power meter (Figure 29). The mean monochromatic flux outgoing from the monochromator is ≈ 55 mW/cm², measured in a wavelength range between 200 and 1000 nm, corresponding to a white light flux incoming on the monochromator ≈ 104 mW/cm² (±5%). This evaluated value is quite close to the incoming AM 1.5 solar light flux at midday for mid-latitudes (≈ 100 mW/cm²). Infrared radiations are filtered just after the lamp output to prevent the next elements from inconvenient heating.

4.2. The PEC cell

This cell is custom-designed to fit a 3-electrode system (a working electrode, a counter electrode, a reference electrode and the electrolyte) and allows solar irradiations to penetrate the cell and shine on the photoactive electrode. The sample is mounted as the working electrode using a dedicated sample holder permitting merely the contact between the NW contained surface and the electrolyte. A platinum (Pt) wire serves as the counter electrode, and an Ag / AgCl electrode as the potential reference. As far as the electrolyte, we used a 0.1 M sodium hydroxide solution (NaOH) (pH = 13) instead of pure water to obtain a better conductivity.

The sample is irradiated through a quartz window by the light flux coming from the lamp modified by the optical chopper and / or the monochromator. The sample is directly shined from the side on which NWs were grown. The electrical contact with the external circuit is realized from the back of the sample (the unpolished side of the Si substrate). All electrochemical measurements were performed at room temperature (RT) inside a black box to prevent all disturbances from the natural light.

4.3. The potentiostat and I-V voltammetry

The potentiostat controls the potential between the working and reference electrodes and measures the current flow between the working and counter electrodes. We used a Princeton Applied Research 263A model. It is controlled by the Power Suite software (dedicated to electrochemistry) or by home-made LabView programs.[13]

The most relevant electroanalytical measurement of this work is the I-V voltammetry. The current is measured as a function of the applied potential. The photocurrent is defined as the difference between the current recorded under light (I_L) and the one without (dark, I_D). In order to increase the signal-to-noise ratio, several I-V curves without illumination and under illumination are recorded and subsequently averaged. To make fair comparisons, current in Ampère is converted into current density J in mA/cm² taking into account the illuminated surface. The photocurrent density is then obtained by $J_{ph} = J_L - J_D$, which is the absolute reply of the working electrode to the illumination. To compare, in spite of J_{ph} one need to also claim the corresponding applied potential. It will be meaningless to compare J_{ph} at different potentials for different samples. Also we can approximately derive the onset potential (the applied potential at which the water electrolysis starts) from the I-V curve.

In this work, I-V measurements were recorded in a potential window from -1 to -0.3 V vs Ag / AgCl (saturated) reference electrode with a scan speed of + 50 mV/s. For the purpose of comparison, it is also worth noting that the relationship among potential vs Ag / AgCl, potential vs SHE (standard hydrogen electrode) and potential vs RHE (reversible hydrogen electrode):

$$\mathbf{V_{SHE} = V_{Ag/AgCl} + 0.197\ V}$$

$$\mathbf{V_{RHE} = V_{SHE} + 0.0592 \times pH}$$

Besides, it is possible to measure J-V curves with an ON-OFF chopped light obtained by an optical chopper. Comparing to a constant illumination, the ON-OFF chopped light clearly shows the illumination effect on the current as well as the transient phenomena which is rather relevant to the reaction kinetics.

4.4. Optical chopper

Generally speaking, the optical chopper is a rotating disc with holes, working as a mechanical shutter for the light beam. It can periodically interrupt the light beam, so the

intensity of light can be manipulated. Hence, the simple optical choppers are widely used in science labs in combination with a lock-in amplifier which is used to improve the signal-to-noise ratio.

4.5. Incident photon to current conversion efficiency

Normalized metrics are required in order to quantify the performance and efficiency of PEC materials and devices. It will also make fair comparisons feasible between different materials and systems. There are several metrics, such as solar-to-hydrogen conversion efficiency (STH), applied bias photon to current conversion efficiency (ABPE), absorbed photon to current conversion efficiency (APCE), and incident photon to current conversion efficiency (IPCE). We focus on the IPCE herein.

The IPCE measures the efficiency of converting an individual photon to an extractable electron. The current density is measured as a function of the wavelength of a monochromatic incident light, while the applied potential is kept constant. IPCE can be calculated via the following formula:

$$IPCE(\lambda) = \frac{electron\ flux}{photon\ flux} = \frac{|\ J_{ph}(mA/cm^2)\ |}{P_\lambda(mW/cm^2) \times \lambda(nm)} \times \frac{hc}{e}(Vm)$$

where J_{ph} is the photocurrent density, P_λ is the power of light at a particular wavelength λ, and λ is the light wavelength; h is the Plank's constant, c is the speed of light, e is the charge of an electron, therefore hc/e can be simplified to 1239.8 Vm.

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Chapter 3. The growth of self-catalyzed GaAs NWs on Si substrate

1. Introduction

III-V compound semiconductors provide the material basis for a number of well-established commercial technologies, as well as new cutting-edge classes of electronic and optoelectronic devices.[1-4] The integration of high-performance III-V semiconductors with the low cost and well developed Si industry has undoubtedly received increasing attentions. Toward the monolithic optoelectronic integrated circuit goal, the hetero-epitaxy of III-V semiconductors, like GaAs, on Si is one approach that has been extensively studied for improving the current problem of the relatively slow rate of data transmission between devices on chips, between systems of circuits, and between circuit boards compared to fast modern processor speeds.[5] However, the lattice mismatch between some III-V semiconductors and Si notably limits the construction and the physical performances of the heterostructure. For example, the lattice mismatch between GaAs and Si is 4.1% at RT, and the resulting high structural defect density (mainly dislocations) degrades the luminescence of GaAs / Si 2D heterostructures.[5] Furthermore, the difference in the thermal expansion coefficients between these two materials accentuatedly hinders the applications and the development of these heterostructures.[6] Strategies like different annealing procedures and the growth of buffer layers are implemented to minimize the dislocation density.[5,7]

In the year of 2004, L. Samuelson group firstly reported the heteroepitaxial growth of III-V SC NWs on Si substrate showing visible RT luminescence,[8] which opened a way to build hetero-systems with new configurations. Due to their nanometric diameter and the efficient strain elastic relaxation at the lateral surface, NWs can accommodate more strain, and thus minimize lattice-matching constraints, which is nearly inevitable in conventional thin film epitaxial growths as we discussed above. After well integrated with Si, III-V- semiconductors-based NW arrays can reach their potentials as the building blocks for electronic and photonic devices due to their ultrahigh specific surface area, effective charge carrier separation and increased light absorption properties.

Before constructing core / shell NWs, the geometry of GaAs NWs serving as the core should be optimized. So in this chapter, we investigated the effect of different experimental MBE parameters on the morphology of self-catalyzed GaAs NW arrays. This first experimental chapter can give a fundamental understanding of the growth mechanism of self-catalyzed GaAs NWs on Si substrates, and also offer a relatively practical guideline for who plans to control the NW morphology.

2. The growth of self-catalyzed GaAs NWs on Si substrate

As discussed in Chapter 1, the self-catalyzed GaAs NWs are grown by MBE using the VLS mechanism with Ga droplets as catalyst. The effect of the Si substrate orientation, the pre-deposition of Ga droplets, the growth temperature, the ratio between the beam equivalent pressure (BEP) of As and Ga ($R_{V/III}$), as well as the growth time will be studied and discussed.

All the Si substrates we used in this chapter are epi-ready n-type Si(111) substrates doped with phosphorus. The dopant concentration is around $10^{18}/cm^3$. The substrates are covered by a native SiO_2 layer with a thickness of around 2 nm which can facilitate the formation of Ga droplets.[9] They were merely ultrasonically cleaned in acetone and then in ethanol, 5 min for each. No other chemical or physical treatment was applied. The SEM side view images were generally taken in a tilting angle of 45°. Only exceptions will be indicated. The sample temperature is measured by a thermocouple and a pyrometer. The relationship between the temperature measured from the thermocouple and from the pyrometer is also established (Chapter 2).

2.1 Effect of the Si substrate orientation

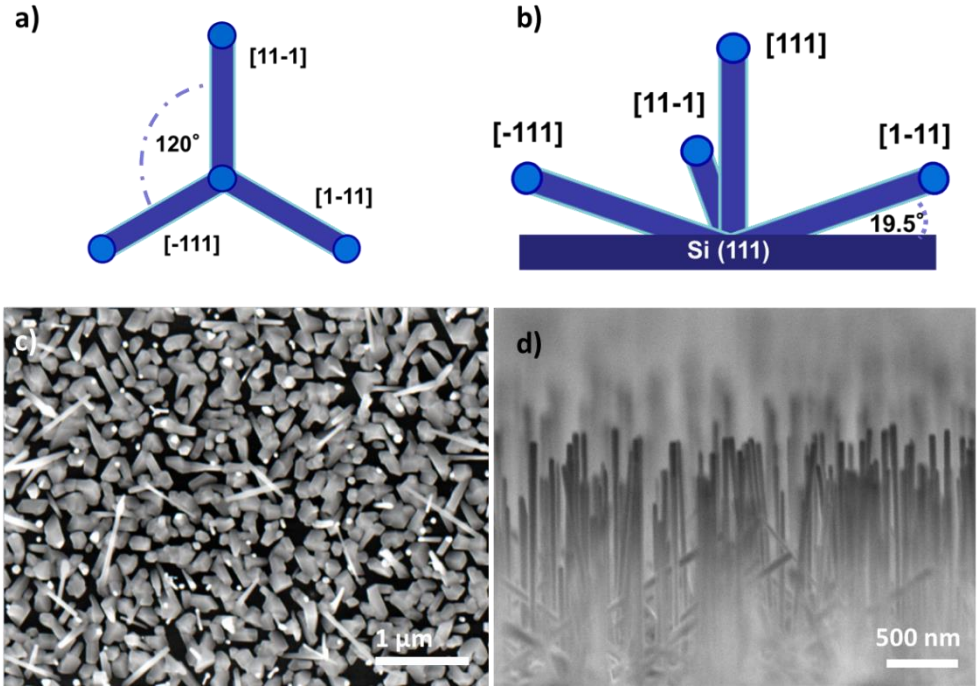

Figure 30. A schematic of a) the top view and b) the side view for the four equivalent <111> NW growth directions on a Si(111) substrate; SEM images of c) the top view and b) the side view (tilting 90°) for an as-grown GaAs NW array on Si(111) substrate. Ga pre-deposition: F_{Ga} = 0.5 ML/s, 2s at 400 °C; NW growth: F_{Ga} = 0.75 ML/s, 10 min at 570 °C, $R_{V/III}$ = 10.

In order to integrate a shell homogeneous in thickness and composition, vertical GaAs NW arrays are preferred. However, the control of the growth direction is far from

straightforward due to the polar nature of binary III-Vs and the non-polar nature of Si substrate.[10] Due to the fact that III-V NWs favor to grow along <111>B directions,[10,11] we started the study from Si(111) substrates. Nevertheless, in addition to the [111] direction, there are three more equivalent growth directions based on its cubic structure, namely [-111], [1-11] and [11-1], shown in more distinct schematics (Figure 30 a, b). The majority of NWs are vertical ones, and the minority inclined (or oblique) NWs are clearly shown in both top and side view SEM images (Figure 30 c, d).

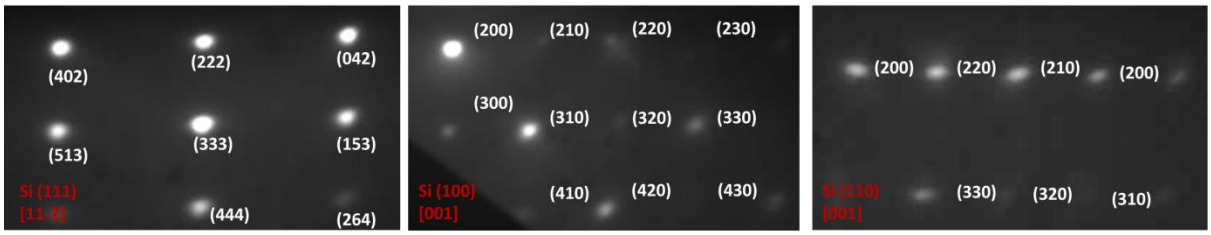

Figure 31. RHEED patterns obtained after the NW growth on: a) Si(111) along [112] azimuth, b) Si(100) along [001] azimuth and c) Si(110) along [001] azimuth. Ga pre-deposition: F_{Ga} = 0.5 ML/s, 2s at 400 °C; NW growth: F_{Ga} = 0.75 ML/s, 10 min at 570 °C, $R_{V/III}$ = 10.

To further confirm the influence of the Si substrate orientation on the growth direction of the NWs, Si(100) and (110) substrates are also investigated. Obviously, the RHEED patterns (Figure 31) are different and characteristic (for a given azimuth) for NW arrays grown on these three different Si substrates. Secondly, it can be seen from SEM images (Figure 32 c, d) that the angle between the NW growth direction and the surface of the Si(100) substrate is around 35°, while it is about 54° for the case of Si(110) substrate. The NWs grow in four different directions on Si(100), and in two on Si(110) (Figure 32 g, h). Thereby, there are four equivalent growth directions on Si(100), namely [-111], [-1-11], [-1-1-1] and [-11-1] (Figure 32 a, e), while only two, [-1-1-1] and [-11-1] (Figure 32 b, f) on Si(110). This revealed that in both cases NWs grew along <111> directions which are indeed the preference for the growth of GaAs NWs, rather, a large variety of III-V semiconductor NWs. Although we didn't get vertical NW arrays by using these two kinds of substrate, the arrays consisting of oblique NWs might also be applied into optical-electrical(-chemical) devices, for example for a better absorption of solar light by lengthening the light path.[12,13]

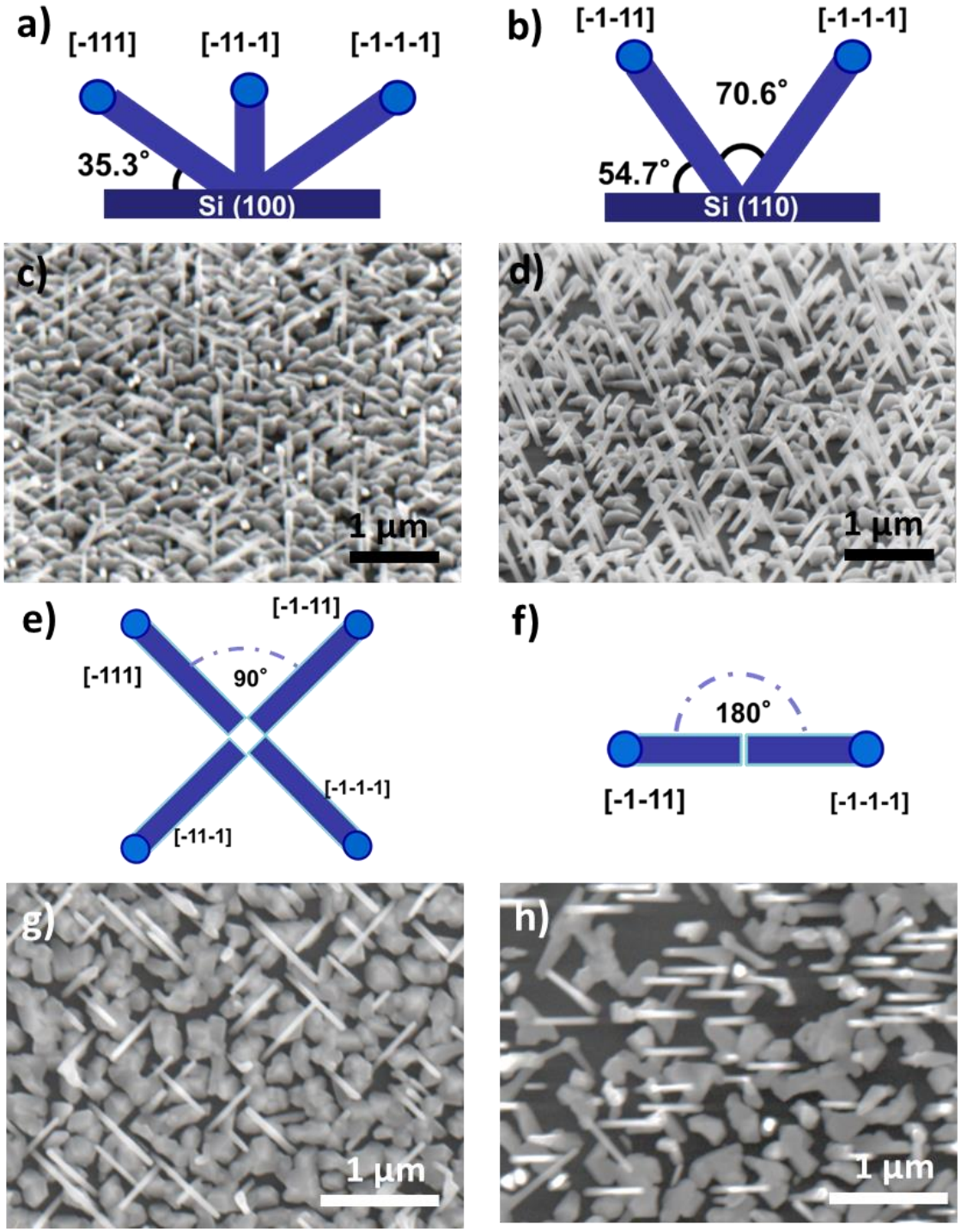

Figure 32. Side view schematics of GaAs NWs growth on a) Si(100) and b) Si(110) substrates; c-d) the corresponding SEM images (tilting 30°). Top view schematics of GaAs NWs growth on e) Si(100) and f) Si(110) substrates; g-h) the corresponding SEM images. Ga pre-deposition: F_{Ga} = 0.5 ML/s, 2s at 400 °C; NW growth: F_{Ga} = 0.75 ML/s, 10 min at 570 °C, $R_{V/III}$ = 10.

2.2 Effect of growth temperature

To explore the effect of the growth temperature, several experiments were done over a temperature range from 490 to 610 °C, with 20 °C for the interval. For this series of experiments, a pre-deposition of Ga was performed at 400 °C with a Ga flux F_{Ga} = 0.5 ML/s and lasted for only 2 s (about 1ML of Ga). After the pre-deposition, it took 8 min to heat the substrate from 400 °C to the given growth temperature via a regulated ramp. The growth time was set to 10 min with F_{Ga} = 0.75 ML/s and $R_{V/III}$ = 10. In some cases, the NW density varied depending on the sample regions. This behaviour might be caused by the inhomogeneity of native SiO_2 and / or by the inhomogeneous heating (the arrangement of the filament and the contact with a sample holder of different thermal conductivity).[14] The SEM top view micrographs (Figure 33 a_1-g_1) allow distinguishing NWs (white or light grey), parasitic crystal islands (middle grey, sharp edges) and uncovered SiO_2 / Si (111) substrate (dark grey or black).

When the growth temperature is low, around 490 °C, the NW density is relatively high (≈ 13 NW/μm^2), but the 3 dimensional (3D) layer consisting of the parasitic crystals of GaAs is thick enough to cover almost the entire surface of the Si substrate (Figure 33 a). The ratio of vertical NWs over the total amount of NWs ($R_{v/t}$) is also relatively high (about 92%, Figure 33 h). The parasitic crystals could be attributed to a 3D growth mode of GaAs on the Si substrate without the assistance of Ga catalyst droplets.

As the growth temperature is increased step by step, the quantity of parasitic crystals as well as the density of NWs decreases, especially from 570 to 610 °C (Figure 33 e-h). From the top view of the sample grown at 570 °C (Figure 33 e_1 insert), the NWs are grown in isolation, confirming their growth from the Si substrate rather than from the GaAs parasitic crystals. The NW density is around 6 NW/μm^2, and the ratio of vertical NWs is about $R_{v/t}$ is about 84% (Figure 33 h). Around 590 °C, NW density decreased to 3.8 NW/μm^2), the $R_{v/t}$ increases to 95% (Figure 33 f, h). The parasitic crystals also vanish, the surface of Si substrate is nearly fully exposed. Interestingly, the shape of the parasitic crystals in Figure 33 f suggests they were formed via the in-plane VLS growth mode under assistance of the Ga droplet which remains in contact with the substrate and the crystal. This in-plane growth mode is well explained in the thesis of S. Breuer.[15] At 610 °C (Figure 33 g_1), the growth of NWs is no longer significant, neither the parasitic crystals. This can be explained by the fact that at this high temperature, Ga evaporates and only few NWs can be initiated via the VLS mode. Besides, the decomposition and evaporation of GaAs should also be considered. Taking into consideration of the NW density, the ratio of vertical NWs and the parasitic GaAs crystals, 570 °C is chosen as the favourable growth temperature for NWs studied in the next chapters.

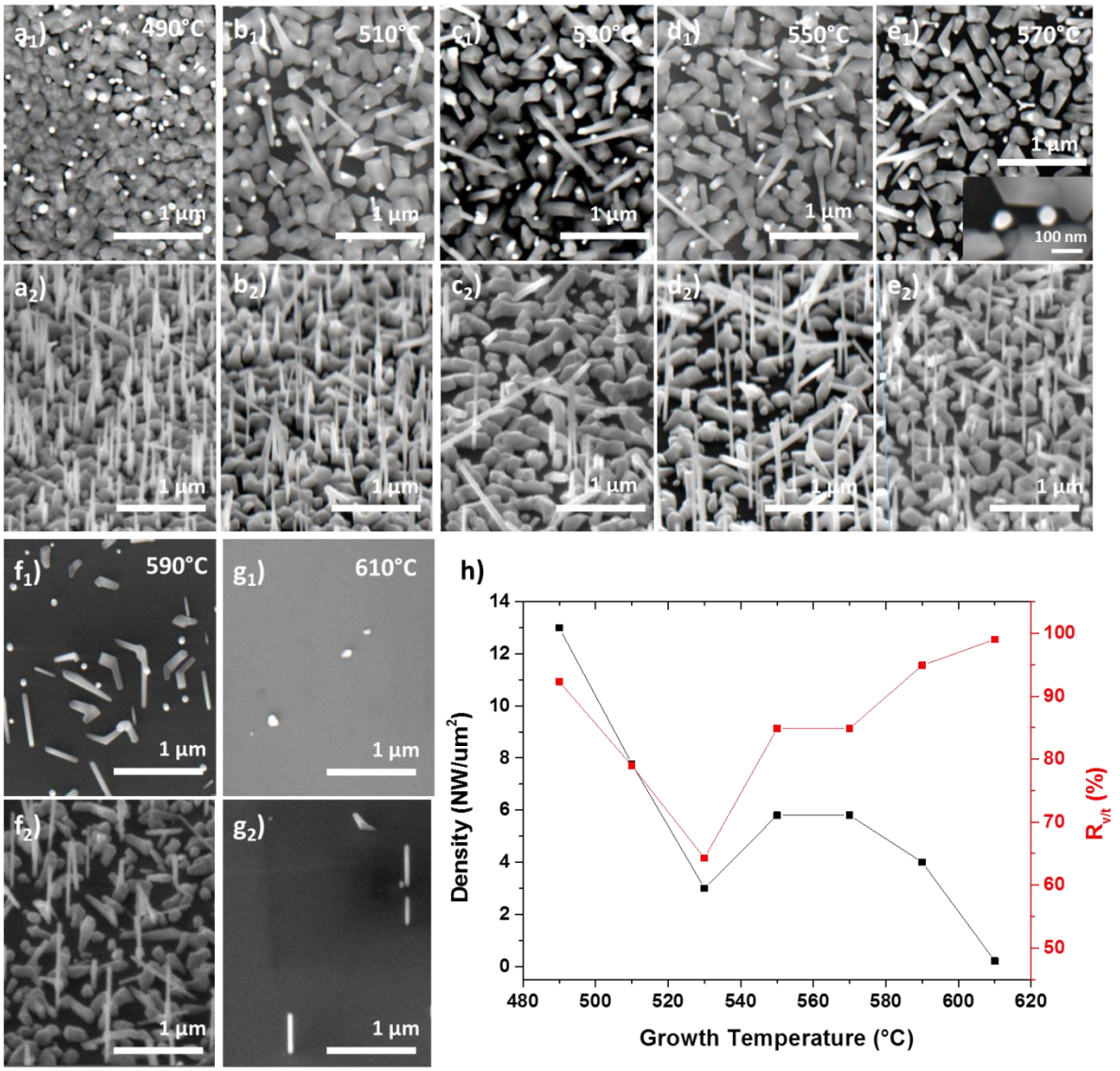

Figure 33. a_1-g_1) SEM top view images; a_2-g_2) SEM side view images; h) The trend curve of density and ratio of vertical NWs for different growth temperatures. Ga pre-deposition: F_{Ga} = 0.5 ML/s, 2 s at 400 °C; NW growth: F_{Ga} = 0.75 ML/s, 10 min at a given temperature from 490 to 610 °C, $R_{V/III}$ = 10.

2.3 Effect of the Ga pre-deposition quantity

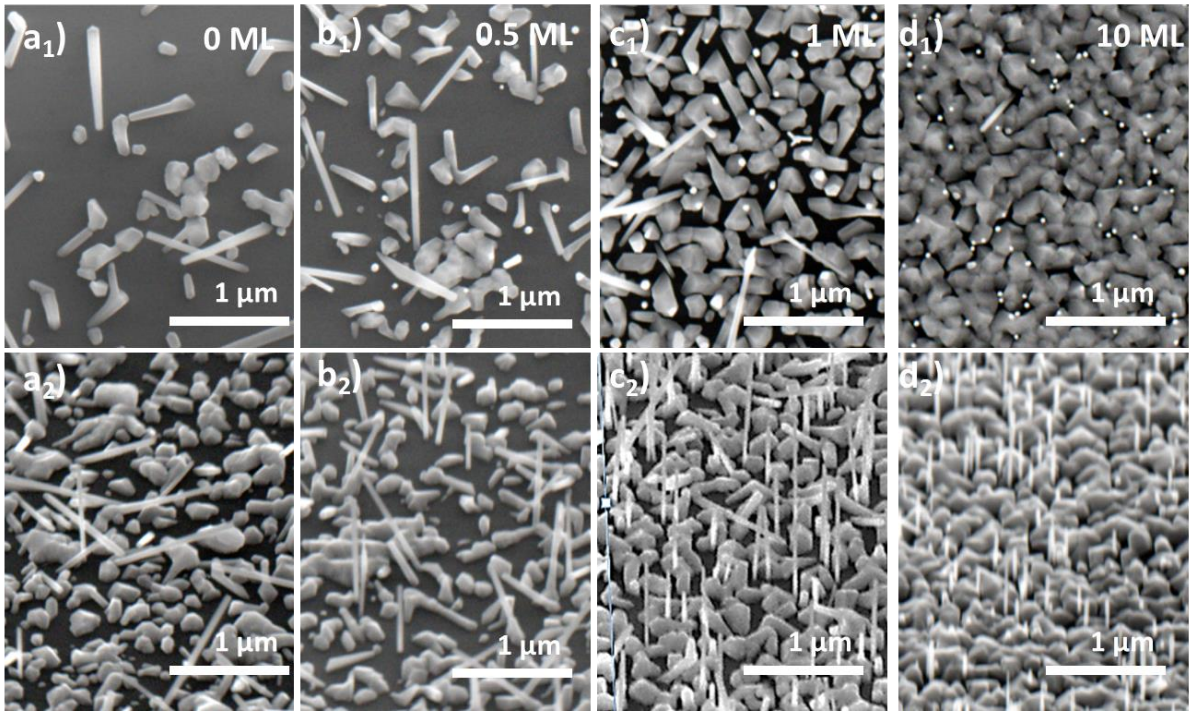

Figure 34. a_1-d_1) SEM top view images and a_2-d_2) SEM side view images for NWs with different Ga pre-deposition quantity. Ga pre-deposition: F_{Ga} = 0.5 ML/s, a given ML of Ga at 450 °C; NW growth: F_{Ga} = 0.75 ML/s, 15 min at 570 °C, $R_{V/III}$ = 10.

Then, the Ga pre-deposition quantity was taken into consideration for a Ga flux F_{Ga} = 0.5 ML/s (1.4 Å/s). Firstly, the pre-deposition step was omitted, which means no holes were formed in the SiO_2 layer in this case (Figure 34 a). A lot of parasitic crystals appear to be on the substrate surface, while there are some oblique NWs and very few vertical NWs. For the one with 0.5 ML of Ga (Figure 34 b), the situation is merely slightly better than the former one but far from sufficient. When we pre-deposited 1 ML of Ga, the NW density notably increased to 6 NW/µm^2 (Figure 34 c, Figure 35), as well as the parasitic GaAs crystals. With 10 MLs of Ga (Figure 34 d), the density rose again, however, NWs are shorter (0.5 µm) and thinner (35 nm) than the one grown with 1 ML of Ga (0.9 µm, about 40 nm) (Figure 35). This could be caused by the fact that 10 ML of Ga creates more pin-holes in the SiO_2 layer leading to a higher density of shorter and thinner NWs. Besides, the 3D layer is even thicker (Figure 34 e) compared to the other samples probably due the consummation of the SiO_2 layer leading to a larger sticking coefficient of Ga and As atoms. Synthesizing the factors like the NWs morphology and the parasitic crystal density, the pre-deposition of 1 ML of Ga has been chosen.

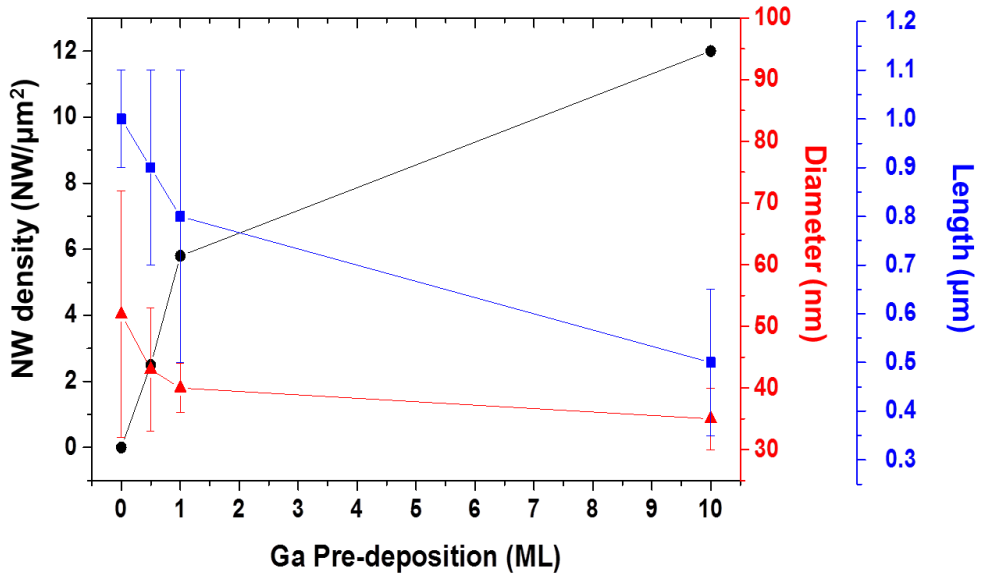

Figure 35. GaAs NW average diameter (red), length (blue) and density (black) as a function of the Ga pre-deposition quantity. Ga pre-deposition: F_{Ga} = 0.5 ML/s, a given ML of Ga at 450 °C; NW growth: F_{Ga} = 0.75 ML/s, 15 min at 570 °C, $R_{V/III}$ = 10.

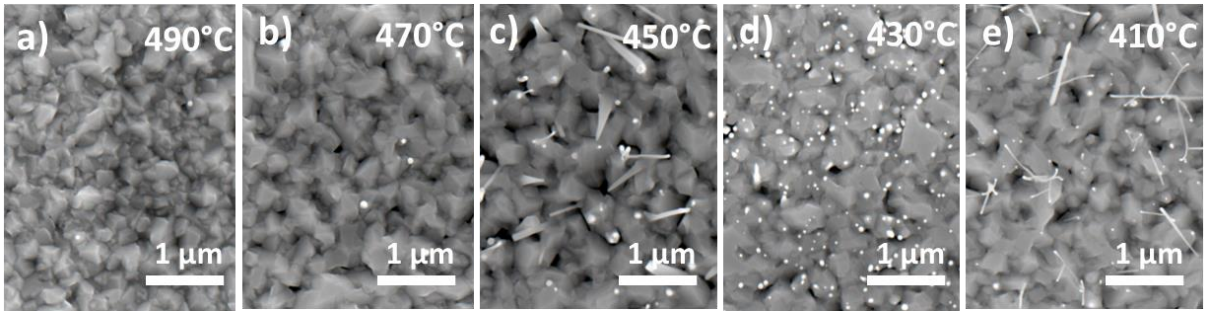

Figure 36. SEM top views of GaAs NWs with different Ga pre-deposition temperatures. Ga pre-deposition: F_{Ga} = 0.5 ML/s, 1ML at a given temperature; NW growth: F_{Ga} = 0.75 ML/s 15 min at 540 °C, $R_{V/III}$ = 20.

Besides the Ga pre-deposition quantity, the substrate temperature is also an important parameter when implementing the pre-deposition step. A series of experiments is also done for studying this effect. For a pre-deposition at 490 °C, there is almost no NW and only the 3D layer can be observed in Figure 36 a. It is supposed that Ga atoms were not sufficiently absorbed on the substrate surface when the substrate temperature was as high as 490 °C.[16] Hence, there are only few holes which can initiate the NW growth. The NW density is slightly higher in the case of the pre-deposition at 470 °C and 450 °C (Figure 36 b, c and Figure 37). Keep decreasing the pre-deposition temperature to 430 °C (Figure 36 d), the NW density reaches a maximum around 16 NW/µm. Indeed, the density decreases again when the Ga pre-deposition was realised at 410 °C (Figure 36 e). Based on the former reports,[17,18] the reaction between Ga and Si oxides, which is very temperature sensitive, occurs at around

600 °C (real temperature as measured by the pyrometer and corresponding to 580 °C in our temperature scale measured by the thermocouple, Chapter 2). From RHEED observations we think that the reaction between Ga and SiO_2 happens in fact around 560 °C measured by the pyrometer and therefore around 510 °C in our temperature scale. Considering now the temperature at which the Ga is pre-deposited we can explained our results as follow: At 490 °C, Ga does not stick very well to the native SiO_2, causing few Ga droplets. Between 470 and 430 °C, Ga sticks better to the surface and thus forms more and more droplets with smaller diameter. At 410 °C, the density of the droplets increases further, their diameter decreases again as well as their volume. We assumed that there is not enough Ga per droplet so that the droplets can not completely reduce the native SiO_2 except at lower thickness locations and thus leading to a lower density of epitaxial NWs (vertical NWs). Taking consideration of the NW density and the NW diameter we chose 450 °C as the pre-deposition temperature.

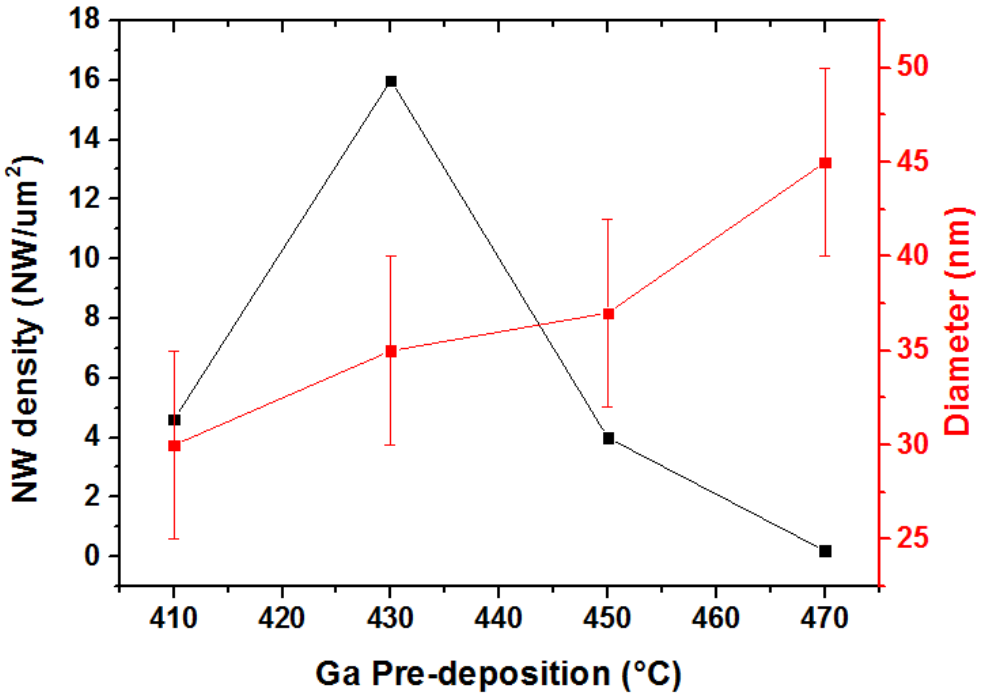

Figure 37. GaAs NW average diameter (red) and density (black) as a function of the Ga pre-deposition temperature. Ga pre-deposition: F_{Ga} = 0.5 ML/s, 1ML at a given temperature; NW growth: F_{Ga} = 0.75 ML/s 15 min at 540 °C, $R_{V/III}$ = 20.

2.4 Effect of the As / Ga pressure ratio

Another important parameter for the III-V NW growth is the pressure ratio between the V and III group elements (noted as $R_{V/III}$), As and Ga in our case. To evaluate the effect of $R_{V/III}$ on the NW growth, three different $R_{V/III}$ are studied, 5, 10 and 20, respectively. For all these three experiments, the As flow was cut during the sample cooling procedure after the 20 min of growth to observe the influence of the $R_{V/III}$ ratio during the growth on the catalyst

droplets at the tip of NWs. As seen from Figure 38 a, the density of NWs is quite low, 0.6 NW/µm^2 (Figure 38 a), for the smaller $R_{V/III}$ of 5. The average NW diameter is 72 ± 10 nm. The parasitic crystals are also evidenced. At the end of almost all NWs, we can observe a round catalyst droplet. Some big droplets are also observed on the top of the 3D layer (marked with the dashed blue square in Figure 38 a).

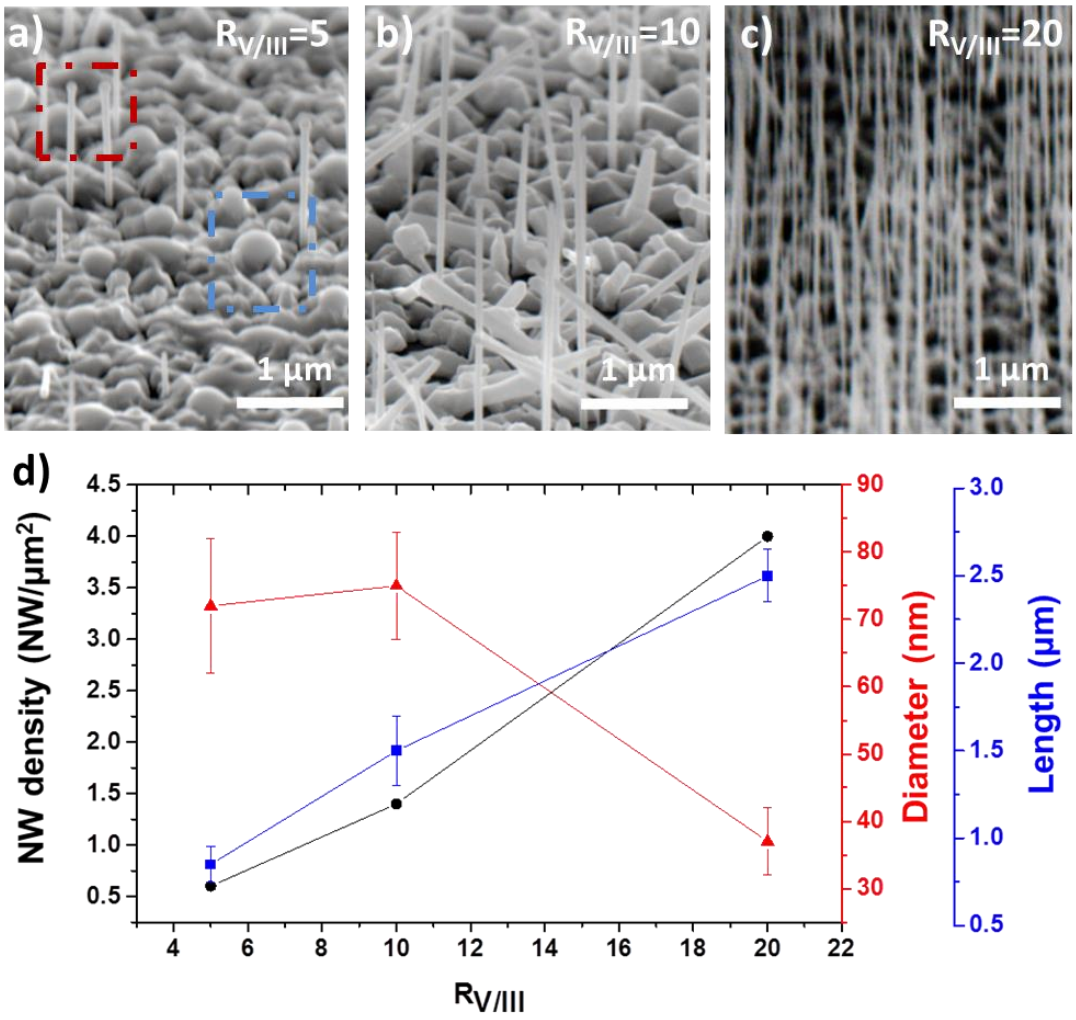

Figure 38. a-c) SEM side view (tilting 30°) images for GaAs NWs grown with different $R_{V/III}$, d) GaAs NW average diameter (red), length (blue) and density (black) as a function of $R_{V/III}$. Ga pre-deposition: F_{Ga} = 0.5 ML/s, 1ML at 450 °C; NW growth: F_{Ga} = 0.75 ML/s, 20 min at 540 °C.

Then, when the $R_{V/III}$ is increased to 20, the NW density is increased to 4 NW/µm^2, while the diameter decreases to 38 nm (Figure 38 d). This result can be explained if we consider the beginning of the NW growth when the Ga and As flux are opened: the surface diffusion of Ga adatoms is lowered when the $R_{V/III}$ ratio is increased, leading to the formation of more Ga droplets with smaller size in the preformed holes, and therefore to a higher density of NWs with smaller diameters. Moreover, we can observe that the Ga droplets are still seen at the tip of the NWs with the $R_{V/III}$ ratio of 10, while with the higher $R_{V/III}$ of 20, no more Ga

droplets is observed (Figure 38 c). The consumption of the Ga droplets during the NW growth could be also an explanation for the NW diameter reduction for higher $R_{V/III}$ ratios. Considering the fact that the NW length increases with the enlargement of $R_{V/III}$, this evolution is well explained by the fact that the self-catalyzed GaAs NW growth is limited by the As flux: the higher the As flux is, the quicker the NWs grow axially.[16,19,20]

2.5 Effect of the NW growth time and the Ga flux incident angle

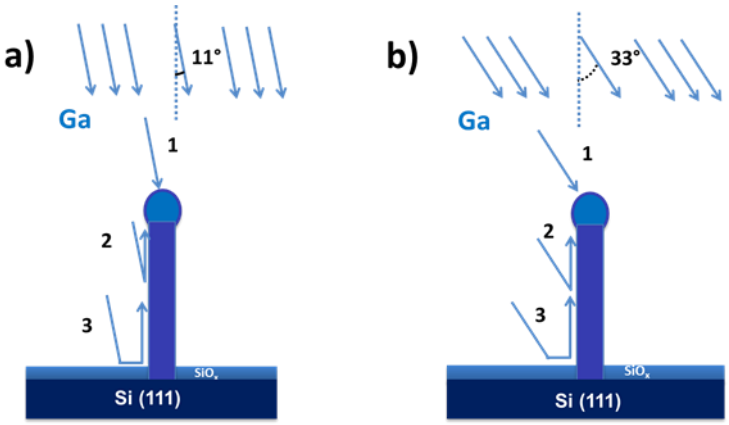

Figure 39. Schematics for the incident Ga atoms during the NW VLS growth, the incident angle of the Ga flux is: a) 11° and b) 33°. Path 1. Ga atoms absorbed directly by the catalyst droplet; path 2. Ga atoms arriving at the facets of the NW and diffusing to the catalyst droplet; path 3. Ga atoms arriving at the surface of the substrate and diffusing to the catalyst droplet.

In order to control the length of the NWs, the growth time was turned from 5 min to 80 min. F_{Ga} was set to 0.75 ML/s (2.1 Å/s) during the growths. The incident angle of the Ga flux was 11° (Figure 39 a). The morphology and the average length of NWs are presented in Figure 40. For a growth time of 80 min, the NWs can reach 7 µm in length (Figure 40 d). During this PhD work, the position of the Ga cell was changed, the new incident angle for Ga flux is 33° (Figure 39 b). For a growth time of 90 min, the NWs can reach 14 µm in length (Figure 40 f). For both cases mentioned above, the oblique NWs are longer than the vertical ones as observed in Figure 40 a-d.

For self-catalyzed GaAs NWs, it is well admitted that the axial growth rate is only limited by the As incorporated in the Ga droplet.[16,19,20] Hence, for a fixed As flux, the length of NW should increase linearly in proportion to the growth time. However, from Figure 40 e, a non linear increase of the NW length is observed for shorter growth times (regime 1), followed by a linear increase for longer ones (regime 2). The "guide to the eye" fitting (Figure 40 e, red dashed line) well illustrates the two growth-regimes as a function of the growth time. This length increase behaviour is similar to that of gold (Au)-catalyzed GaAs NWs,[21-23] of which the axial growth rate is limited by both Ga and As incorporations in the Au-droplet.

The growth time effect on the length of Au-catalyzed NWs are explained by considering 1) the Ga atoms contributing to the feeding of the Au droplet during the growth and 2) the diffusion length of the Ga adatoms (denoted as λ_{Ga}, the average length that the Ga adatoms can diffuse on a surface before being incorporated or desorbed). The most effective way for Ga atoms to participate in the VLS growth is to meet the Au droplet directly (Figure 39, path 1). Ga adatoms can also be involved in the growth via the diffusion along NW facets (Figure 39, path 2 and 3). The NW facet surface area increases with the NW elongation. When the NW length is smaller than λ_{Ga}, the longer NWs are, the more adatoms can be acquired and thus more adatoms are able to diffuse to the Au droplet to participate in the VLS growth, leading to a non linear increase of the NW length with the growth time (similar to the length increase behaviour shown in Figure 40 e regime 1). Once the NW height exceeds λ_{Ga}, the number of Ga adatoms participating in the VLS growth becomes independent of the NW length and a linear length increase is observed (similar to Figure 40 e regime 2).

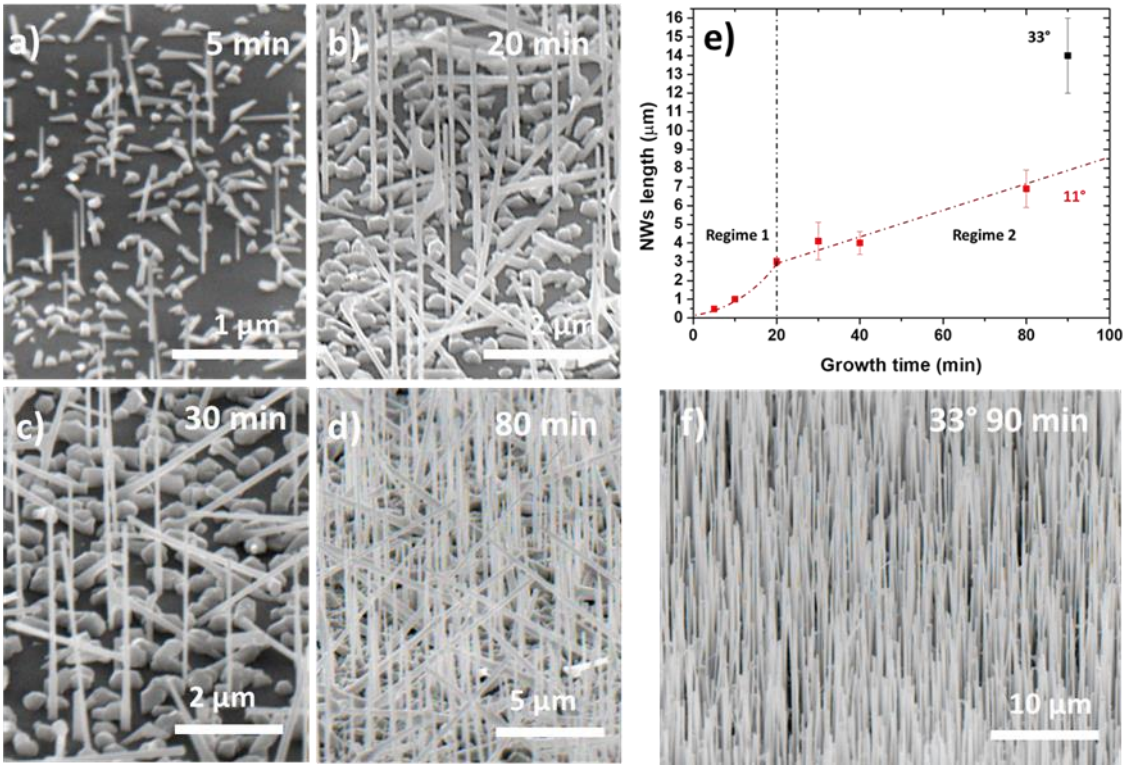

Figure 40. a-d) SEM side view (tilting 30°) images for NWs with different growth times, the incident angle for the Ga flux is 11°; e) GaAs NW length as a function of the growth time, dashed red line is a guide to the eye; f) SEM side view image for NWs grown in 90 min, the incident angle for Ga flux being 33°.

Therefore, the observed length evolution with the growth time as shown in Figure 40 e (if it is true, what remains to be confirmed experimentally) may indicate that the Ga flux arriving at the Ga droplet by diffusion via the NW facets can also play a role in the axial growth of the self-catalyzed GaAs NWs according to assumed mechanisms (increase of the

equilibrium volume of the Ga droplet leading to an increase of the As capture surface, others,…).

With the same considerations, it would be therefore possible to understand that after enlarging the incident angle of the Ga flux to 33° (Figure 39 b), the axial growth rate of vertical NWs is notably increased (Figure 40 f), as its lateral facets can acquire more Ga adatoms which can diffuse to the Ga droplet.

3. The characterization of the optimized GaAs NWs

After all analyzes in the former section, we finally studied the crystal structure of the optimized GaAs NWs. For a typical procedure, the n-type Si(111) substrate with a native SiO_2 is ultrasonically cleaned in acetone and ethanol, 5 min for each. Then the substrate is loaded and degassed at 200 °C in UHV about 10 min. The substrate is transferred in the MBE chamber and heated to 450 °C and 1 ML of Ga is deposited with a Ga flux of 0.5 ML/s (1.4 Å/s). Afterward, the substrate temperature is increased up to 570 °C in 8 min. The As valve is opened 10 s before growth to establish a stable As_4 supply. Then, the Ga cell is opened to initiate the growth of NWs. The Ga flux is 0.75 ML/s (2.1 Å/s) and the As_4 BEP is set as 3.3 x 10^{-6} Torr corresponding to an As flux of 1.1 ML/s (3 Å/s) measured under an As-limited growth condition.[24] 15 min later, the Ga shutter is closed and the sample is cooled down to RT under identical As_4 BEP. This under-As pressure cooling is used to avoid the decomposition of GaAs during the cooling procedure. It also leads to a final GaAs segment growing with the consumption of the Ga droplets under the As flux.

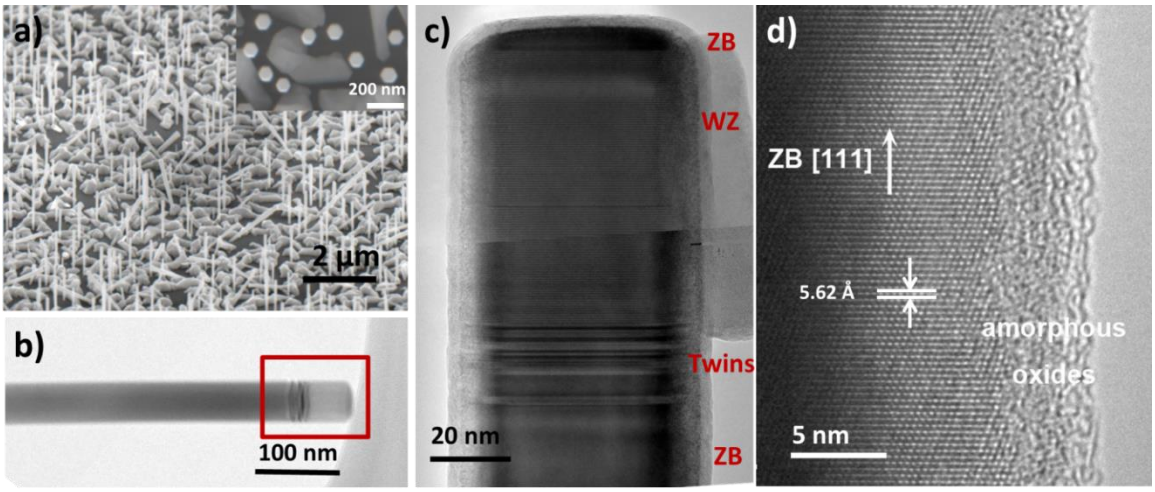

Figure 41. a) SEM side view (tilted 30°) image of the GaAs NWs grown on Si (111) substrate, the inset is its corresponding top view; b) TEM image of a typical GaAs NW; c) TEM image of a GaAs NW tip marked by the red square in b) under higher magnification; d) HRTEM image taken from the first ZB phase of a GaAs NW.

A representative SEM image of the sample is shown in Figure 41 a. The NWs are mainly vertical, with an approximate length of 1.0 µm. The NW density is about 5.5 NW/µm^2. GaAs NWs have an average diameter of 50 ± 10 nm with small inverse-tapering effect. The Ga catalyst is no longer visible at the NW tip. GaAs parasitic crystals are also observed between the NWs. The SEM top view image of the NWs (inset in Figure 41 a) displays that the NWs have a perfect hexagonal cross section. The six facets could be indexed to {1-10} planes, which is common for self-catalyzed III-V NWs grown on Si(111) substrates. Moreover, the facets are systematically aligned with the Si {1-10} planes. The following epitaxial alignment between GaAs NWs and a Si(111) substrate is deduced: GaAs[111] // Si[111] and GaAs[1-10] // Si[1-10], in correspondence with XRD results which will be discussed later.

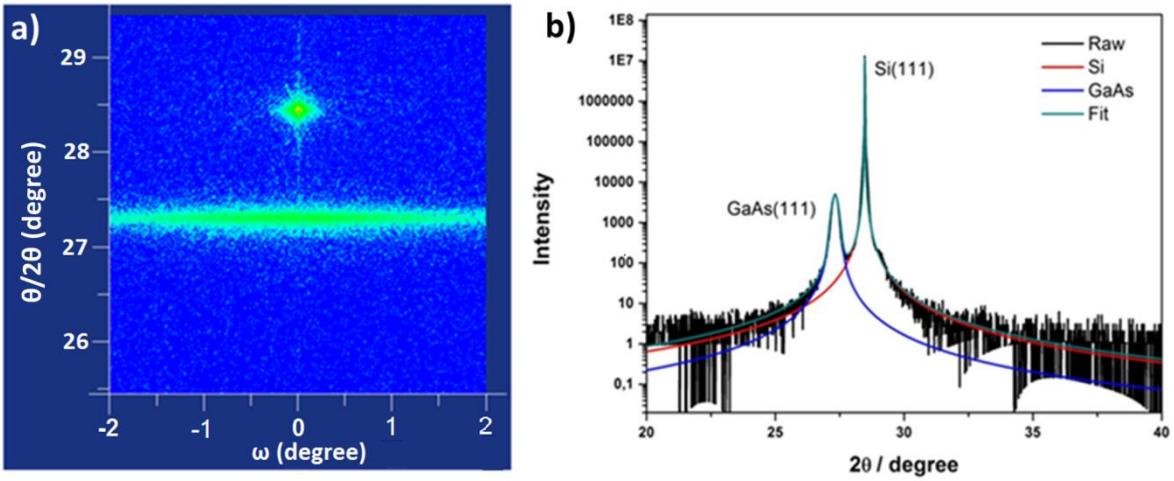

Figure 42. XRD measurements obtained on a GaAs NW array on Si(111) substrate, a) The reciprocal space mapping and b) θ / 2θ scan.

TEM images of GaAs NWs are shown in Figure 41 b and c. The GaAs NW in Figure 41 b is quite representative of the other NWs observed for this sample. Under a higher magnification (Figure 41 c), the NW exhibits four different domains. From the bottom to the top, the first one is a pure ZB phase with only few twins observed all along the NW. The second domain, about 30 nm in length, is located at roughly a hundred nm away from the NW tip. This domain is a transition region with a high density of twins and stacking faults. The following one is a pure WZ phase, around 80 nm in length, the existence of whom is also confirmed by XRD measurements discussed later. And finally, NW ends up into a very thin ZB domain. Such a domain sequence is a consequence of the evolution of the Ga droplet shape when they crystallize under the As_4 flux during the sample cooling, which has already been observed and well explained.[11,25-29] Figure 41 d shows a high resolution TEM (HRTEM) image of a GaAs NW taken from the pure ZB domain. The lattice parameter measured along the NW growth direction is about 5.62 Å, approximately equal to that of bulk GaAs in cubic ZB phase (5.65 Å). Hence, the NW growth axis is deduced as [111] and the zone axis is close to [1-10]. A thin amorphous layer is observed on the NW facet which corresponds to GaAs related oxides formed by the uncontrollable oxidation during the sample transfer to the microscope. It would be critical for the growth of the epitaxial crystalline shell, which will be discussed in detail in chapter 4.

Complementary to the local microstructure analysis by TEM, the NW structure was analyzed by XRD. Figure 42 a shows the reciprocal space mapping of a typical GaAs NW array grown on a Si(111) substrate, measured around the Si(111) and GaAs(111) reflections. The θ/2θ scan in Figure 42 b shows a peak at 28.43 degree indexed to Si(111) which is intense and narrow, as expected for a Si(111) substrate. The GaAs(111) peak, located at 27.32 degree (Figure 42 b), is in good agreement with bulk GaAs, showing the full relaxation of the GaAs lattice in the NWs. Besides, the GaAs(111) peak is narrow along the radial direction (θ /

2θ) and broadened along the rocking angle (ω), which is in accordance with NWs grown epitaxially. Based on the Scherrer equation, the average crystal size is about 49 nm.

Another reciprocal space mapping was performed on this GaAs NW array in order to observe the presence of WZ and ZB phases within the as-grown GaAs NWs. By modifying the incidence angle and the detection angle at a fixed azimuthal angle, the reciprocal space was mapped without moving the sample, allowing the observation of ZB{422}, ZB{331} and WZ{1-105} Bragg spots.[30] These spots are displayed in Figure 43 a, from the bottom to the top of the map, respectively. Another intense Bragg spot close to the WZ[1-105] reflection is assigned to the Si(111) substrate. The map in Figure 43 a allows to extract the in-plane and the out-of-plane lattice parameters of both ZB and WZ phases. The measured lattice parameters confirm the presence of a bulk-like ZB structure (fully relaxed) while the WZ phase exhibits a modification of the out-of-plane lattice parameter c = 6.5696 Å (for bulk WZ c = 6.407 Å) corresponding to a c/a ratio of 1.645, in good agreement with previous literature.[30-32]

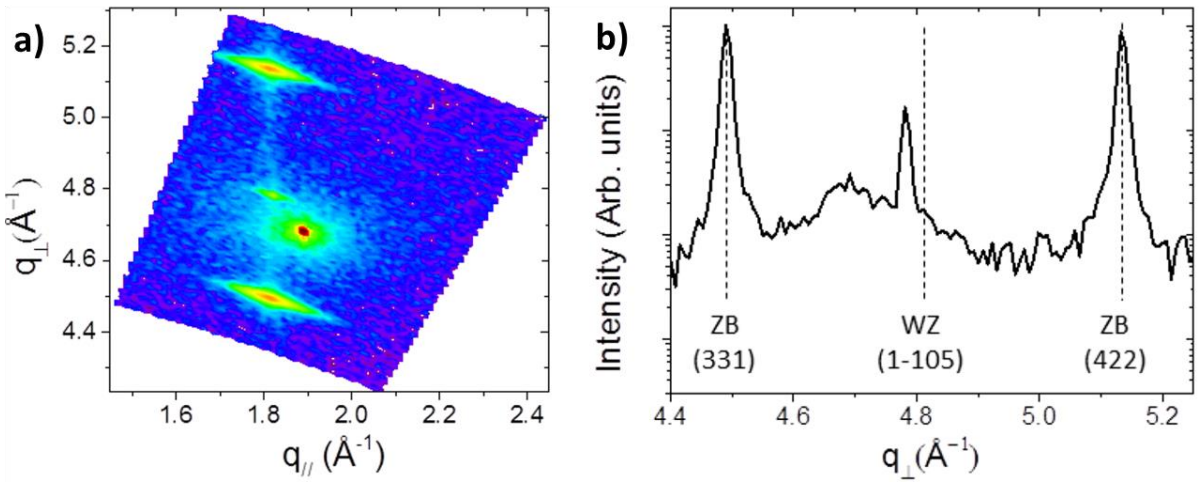

Figure 43. a) The reciprocal space mapping and b) the diffraction intensity plotted along the out of plane scattering vector. The diffuse scattering of the Si substrate is visible close to the WZ(1-105) peak.

4. RHEED study of the GaAs NW structure evolution

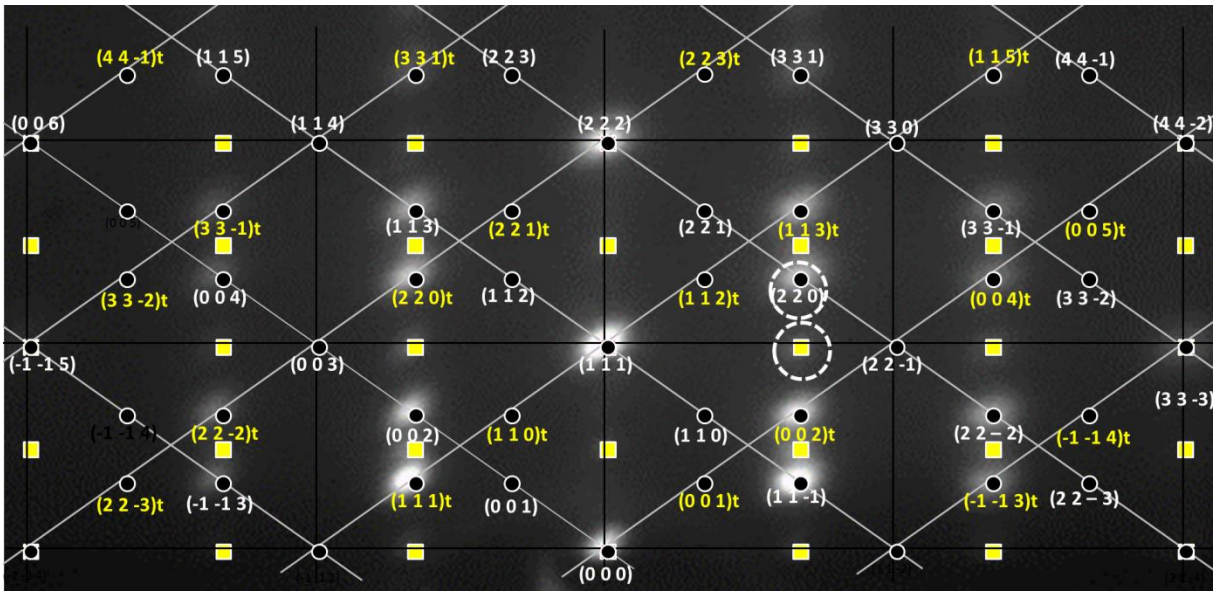

Figure 44. RHEED pattern recorded along of the [1-10] azimuth with a diagram indexation,[33,34] black dots report the ZB plans taking into account the twinned ZB variants, yellow squares report the WZ plans. Some of the diffraction spots disappear due to an extinction of the structure factor F_{hkl}. White circles represent the spots whose intensity is measured to determine the presence of the ZB and WZ phases (mainly at or near the NW top) during the growth.

As discussed, the ZB / WZ sequences are very common for GaAs NWs grown via the self-catalyzed mode in MBE. Since GaAs in different crystalline structures presents different features, especially in photoluminescence, a study on the structure control of GaAs NWs can be rather important. The *in-situ* RHEED diffraction makes this study efficiently feasible. This study was carried out within the framework of Thomas Dursap's internship project.[34] Only the method used for monitoring the structure of GaAs NWs during growth using *in-situ* RHEED diffraction is recalled here.

The GaAs NWs were grown at 570 °C with an As_4 BEP of 5.1 x 10^{-6} Torr and a Ga flux of 0.75 ML/s corresponding to a Ga BEP of 2.9 x 10^{-7} Torr to maintain a $R_{V/III}$ ratio close to 17.5. 1 ML of Ga was pre-deposited at 450 °C to form the Ga droplets. The RHEED pattern was recorded as the video during a typical growth. A diagram indexation of the ZB and WZ phases is given in Figure 44. One specific diffraction spot of the ZB phase and one of the WZ phase, marked with the white circles in Figure 44, were traced to study the corresponding intensity change as a function of growth time.

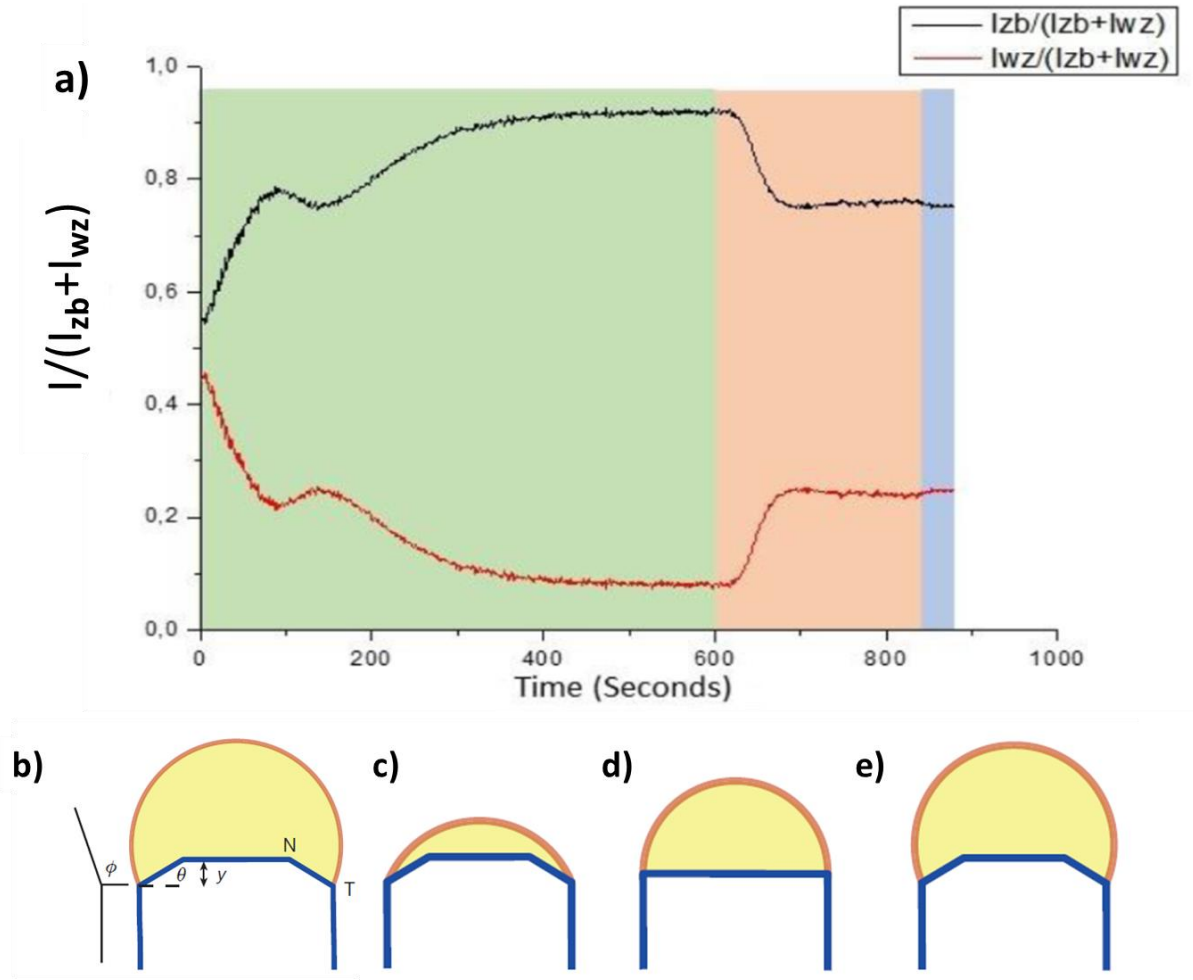

Figure 45. a) Intensity ratio $I_{(zb \text{ or } wz)}/(I_{zb}+I_{wz})$ as a function of the growth time. In green zone the growth is under Ga and As flux, in red the growth is only under As flux and in blue is the sample cooling. b) Schematic of a quasi-two-dimensional, ideal, symmetric nanowire illustrating the droplet contact angle ϕ, and the edge facet angle θ and length (in the growth direction) y. 'N' marks the interior point at which ZB phase nucleates; 'T' marks TPL at which WZ phase nucleates. c-e) Schematics of NW and droplet for c) $\phi < 90°$, d) $\phi = 90°$ and e) $\phi > 90°$.[29]

Figure 45 a reports the intensity ratio $I_{(zb \text{ or } wz)}/(I_{zb}+I_{wz})$, where I_{zb} and I_{wz} are the respective intensity of the ZB and WZ spots, as a function of the growth time. The green area corresponds to the growth under the Ga and As flux. At the time where t = 0 s, WZ and ZB are supposed to be equal to 0.5, due to the absence of NWs. The difference observed is due to the non-homogeneity of the Si diffraction line intensity. An increase of the ZB intensity is observed in the beginning of the growth, followed by a growth phase with a constant value close to 1, which means that the NWs are quasi-entirely ZB at this growth phase. We can note a short increase of the WZ intensity, with corresponding short decrease of the ZB intensity, indicative of a short WZ growth phase after the beginning of the growth. After 600 s of growth, the Ga flux was cut. About 25 s later, we observe an increase of the WZ intensity and a corresponding decrease of the ZB intensity. Based on the recent work reported by D. Jacobsson *et al.*,[29] the switch between phases suggests a scenario in which the growth

conditions (here, the V/III ratio) determine the volume of the droplet which directly affect the aspect ratio h/d and contact angle ϕ of the catalyst droplet (see Figure 45 b). When ϕ > 90°, the front of the NW appears faceted (Figure 45 e). The nucleation occurs at point N (Figure 45 b), and a pure ZB phase is obtained agreeing with the increasing I_{zb} / (I_{zb}+I_{wz} showed in Figure 45 a. When the droplet shrink to ϕ = 90° (Figure 45 d), the front of the NW becomes plane (no edge facet) and the WZ phase states nucleating at the TPL. It lasted for 50 more seconds based on the RHEED pattern in our case. Then droplet continues to decrease, ϕ < 90°, the front of NW turns to faceted again (Figure 45 c), the ZB section is thus regained. The time lag of about 25 s between when the Ga shutter is closed and when the pure-WZ structure started to grow is an evidence of the transition (ZB + WZ) section.

In summary, based on the RHEED monitoring, it is possible to follow the NW crystal structure during the growth. By exploiting this result, it is possible to control the droplet volume and the contact angle which seems to be crucial to the crystal structure and in turn control the growth of self-catalyzed GaAs NWs.

5. Conclusion

To draw a conclusion, self-catalyzed GaAs NW arrays with a good verticality were successfully fabricated on Si(111) substrates by ss-MBE. The morphology of NWs is uniform, about 50 nm in diameter and 1 µm in length, and the NW surface density is as high as 5.5 NW/µm^2. To obtain a better understanding of the growth mechanism, the effect of different experimental parameters were investigated, including the effect of the Si substrate, the Ga catalyst pre-deposition temperature and time, the temperature and time for the growth, as well as the $R_{V/III}$ ratio. The epitaxial growth relationship between the GaAs NWs and the Si(111) substrate is revealed through the XRD reciprocal space mapping. Furthermore, the crystal structure of GaAs NW is studied by TEM and XRD measurements. Both ZB and WZ structures are observed, which is in accordance with the Ga droplet shape evolution during the VLS growth mode.[29,35,36] With the help of the *in-situ* RHEED in MBE, the crystal structure control of GaAs NWs is also feasible.

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Chapter 4. The reversible As-capping method against the uncontrolled oxidation of the NW surface

1. Introduction

Up till now, most of the published works on semiconductor core / shell NWs concern semiconductors of the same family,[1-4] the fabrication of highly heterogeneous shell, such as a functional oxide or a metal shell, on group IV or III-V semiconducting NWs is still challenging.[5] One of the difficulties to overcome arises from the *ex-situ* growth procedure, since MBE reactors are usually equipped with a limited kind of cells and most of the III-V MBE facilities do not permit the sample transfer under UHV conditions between separate reactors for growing a heterogeneous shell. Hence, during the transfer, an uncontrolled oxidation and / or contamination of the III-V NW facets is unavoidable. Unfortunately, because of the nanoscale-size and high specific surface area of NWs, this uncontrolled oxidation and / or contamination could be fatal towards the physical properties of such heterogeneous system. The wet chemical treatment[6] and the atomic hydrogen etching[7,8] are usually applied to obtain clean GaAs NW facets before implementing the shell growth. Nevertheless, such strategies suffer several disadvantages like introducing contaminations from solvents and surface modifications caused by the etching. To preserve the NW surface structure and chemistry, a contamination-free and reversible surface protection would be preferable.

Reversible As-capping / decapping method (named As-cap methods) has been carried out to protect thin films[9-13] and some 1D NWs.[14-17] However, as far as we know, none of the reports clearly elucidated the efficiency of the As-cap method and / or its influence on the structural and chemical properties of the treated surfaces. But, this method could indeed serve as a general strategy for protecting the surface of III-V NWs therefore facilitating an epitaxial shell growth in various deposition reactors equipped with a heating sample holder (MBE, CVD, *etc.*). The growth of metallic, functional oxide or other semiconductor shell on III-V NWs with a controlled interface would then be feasible.

In this chapter, we systematically studied the surface oxidation of GaAs NWs and its negative effect on the subsequent shell growth. Then, the efficiency of the As-cap method was displayed. The analyses highlight the benefit of the As-cap method for: i) protecting GaAs NWs against air exposure inducing surface oxidation and ii) achieving the growth of an epitaxial shell.[18] The main content of this chapter is well illustrated through the schematic presented in Figure 46. All the GaAs NWs used in this chapter were fabricated via the optimized growth procedure based on the study in Chapter 3. The corresponding recipe is given in Chapter 2.

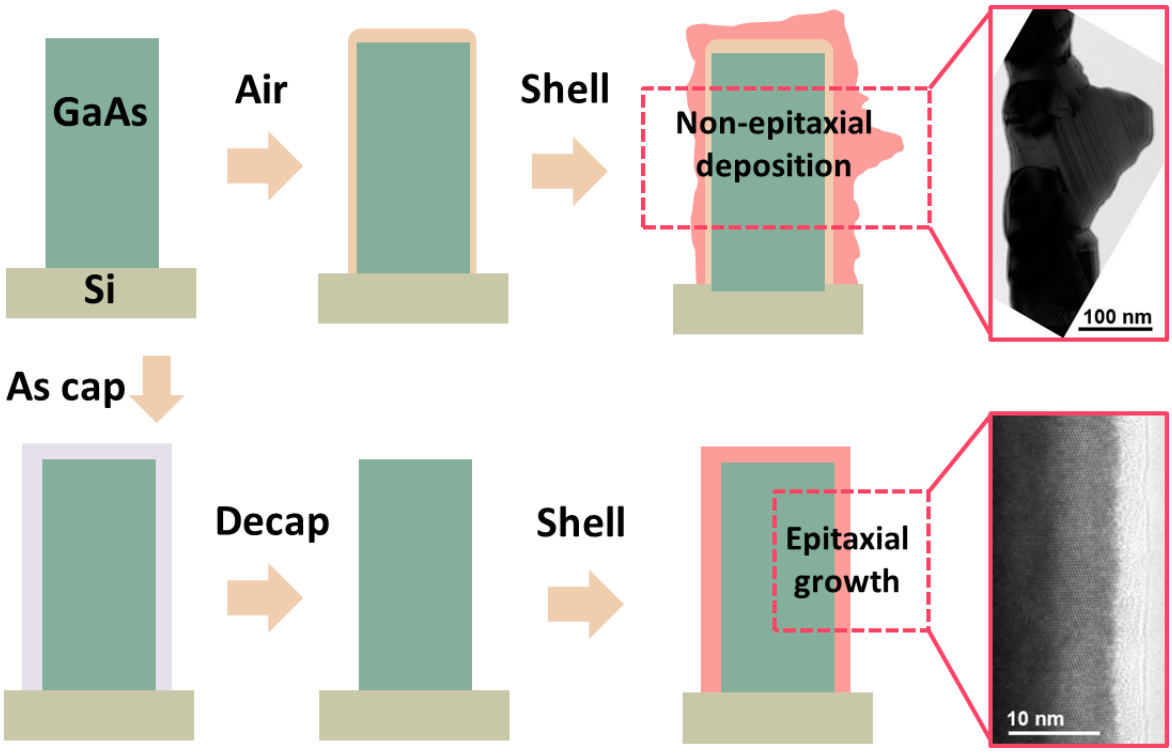

Figure 46. Schematics of the surface oxidation of GaAs NW leading to a non-epitaxial growth of the shell and of the reversible As-cap method facilitating the growth of an epitaxial shell.

2. Surface oxidation of GaAs

Aiming for the construction of an epitaxial heterogeneous core / shell NWs, a relatively clean and abrupt interface is required. As aforementioned in Chapter 3, after air-exposure, an amorphous oxide layer is observed around the GaAs NWs, which could be the obstacle to an epitaxial shell growth and the further performance improvement. Before working on the oxidation-proof method, the study on the composition of the surface oxidation of GaAs NWs is rather necessary.

Using XPS, the surface chemistry of oxidized GaAs NWs is thoroughly studied. First, to acquire a reference spectrum, a newly fabricated GaAs NW array was transferred directly to the XPS chamber under UHV conditions. In the course of this whole process, the sample wasn't exposed to air to prevent the presence of contaminations or oxidation. As shown in Figure 47 row I, the deconvoluted As $3d_{5/2}$ peak locates at 41.0 eV and the Ga $3d_{5/2}$ peak at 19.1 eV, which corresponds to the positions and the stoichiometry expected for bulk GaAs.[19,20] Thanks to the UHV conditions, the symmetric O 1s core level spectrum at 533 eV should originate only from SiO_x, the native oxide on the surface of the n-Si (111) substrate.

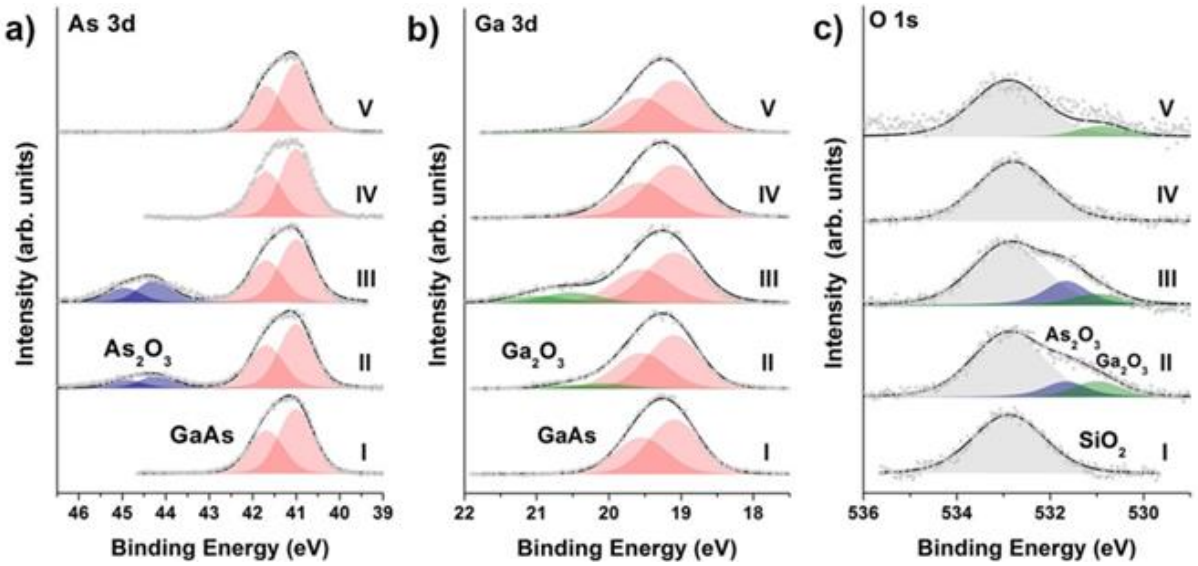

Figure 47. XPS spectra of a) As 3d, b) Ga 3d and c) O 1s core levels of different NW arrays grown on Si(111). I: as-grown GaAs NWs without contact with ambient air; II: GaAs NWs without As-cap stored in ambient air for 24 h; III: GaAs NWs without As-cap stored in ambient air for 1 month; IV: GaAs NWs with As-cap kept in ambient air for 24 h and then decapped; V: GaAs NWs with As-cap kept in ambient air for 2 months and then decapped.

In order to display the time-dependence of the NW oxidation, two GaAs NW arrays were stored in ambient air at room temperature (RT), one for 24 hours (Figure 47 row II) and the other for as long as 1 month (Figure 47 row III), without any other chemical or physical treatment. For the sample with 24 h air-exposure, the As 3d core level (Figure 47 row II) exhibits a supplementary doublet at higher BE (44.3 eV), which can be attributed to the emergent As_2O_3.[19] The Ga 3d core level is also modified and fitted with two more peaks at 20.75 and 20.30 eV, in accordance with the Ga $3d_{3/2}$ and $3d_{5/2}$ of Ga_2O_3,[21] respectively. The O 1s peak (Figure 47c row II) is broadened and asymmetrical due to the appearance of two other oxides, namely As_2O_3 and Ga_2O_3.[22] When the air-exposure time was prolonged to 1 month, the intensity of As(As_2O_3) and Ga(Ga_2O_3) peaks is notably increased (Figure 47 row III). Regarding the O 1s core level, the intensity of components related to As_2O_3 and Ga_2O_3 enhanced as well in proportion to the air-exposure time (Figure 47 c row III). The thermal stability of the oxides was probed by measuring the Ga 3d and As 3d core levels during annealing inside a XPS analysis chamber under UHV at Synchrotron Soleil, indicating a better stability of the Ga oxides compared to the As ones, as also evidenced in former reports.[23,24] More details about the thermal stability will be discussed in chapter 5.

B. Loitsch *et al.* proposed an *in-situ* annealing procedure for getting thin NWs with unoxidized facets.[25] The Ga and As evaporation rates were well controlled to be congruent at 680 °C. However, if NWs are already oxidized, with As oxides and Ga oxides on the surface, the case could be different. Firstly, based on the result of XPS (Figure 47), we have shown that the quantity of As oxides and Ga oxides is different. And their thermal stability are

different too. It is difficult to keep decomposition behaviour for As oxides and Ga oxides the same. So the stoichiometry and the morphology of the de-oxidized GaAs (1-10) NW facets could be different comparing to an as-grown one. Secondly, recent works of our group show that the decomposition rate is not identical for WZ GaAs and ZB one. Since the as-prepared GaAs NWs are not monocrystalline, the surface of NW is obviously roughened during annealing process. In summary, the annealing method might impede the subsequent shell growth. A contamination-free and reversible surface protection would be preferable to well preserve the NW surface structure and chemistry.

3. The reversible As capping / decapping method

The protective As capping layer was grown on the GaAs NWs within the same MBE chamber for the GaAs NW growth. The cracker for As was heated to 920 °C to provide As_2 flux instead of As_4. The As capping procedure was initiated once the NW sample was cooled to 160 °C to prevent the desorption of the As-cap layer at higher temperatures. Rather than a smooth surface of the typical GaAs NWs (Figure 48 b), the newly fabricated surface of As-capped NWs is rough and the As-cap layer is amorphous, as revealed by the TEM image and RHEED pattern (Figure 48 f, g). NWs are thickened from 40 to 75 nm in diameter after a 2 h-capping process (Figure 48 a, b, e and f). EDX elemental mapping (Figure 49) confirms the formation of the As-cap layer and well displays that the core is perfectly wrapped by the As layer. Comparing to As and Ga 3d core levels of pristine GaAs NW shown in Figure 48 d, the As 3d peak in Figure 48 h slightly shifts towards higher BE (0.3 eV). It is indexed to elemental As rather than As in GaAs, as the fact that the photoelectron mean free path of As in GaAs is shorter than the thickness of the As layer. This also explains that Ga 3d core level was not detected in Figure 48 h.

The heating treatment under UHV was applied to the capped NW array inside the MBE chamber to remove the As-cap layer. We termed this procedure as “decapping”. The whole process was monitored by the *in-situ* RHEED. We progressively heated the sample from RT to 440 °C. Correspondingly, the RHEED pattern taken from the same azimuth changed gradually from a continuous bright background (Figure 48 g) to a spotty pattern (Figure 48 k). The final pattern (Figure 48 k) is almost as same as the one of pristine GaAs NW array (Figure 48 c). Both of them reveal a highly twinned ZB structure with also WZ crystal signatures, consistent with the structure of upper part of the NW shown by TEM results in Chapter 3. It also illustrates that the As-cap layer was completely removed and that the GaAs crystal structure was not modified during this moderate annealing process. The TEM image in Figure 48 j shows that the NW regained the smooth facets and returned to the initial diameter of 40 nm. Neither NW structure nor morphology changes occurred after the As decapping procedure. Furthermore, we compared the Ga 3d and As 3d core level spectra of as-grown GaAs NWs, that of capped NWs and decapped NWs (Figure 48 d, h and l). The Ga peak disappears and then re-emerges, and the peak of As 3d core level shifts firstly to higher BE then back to the lower BE side. Both reveal the reversibility of the As-cap method.

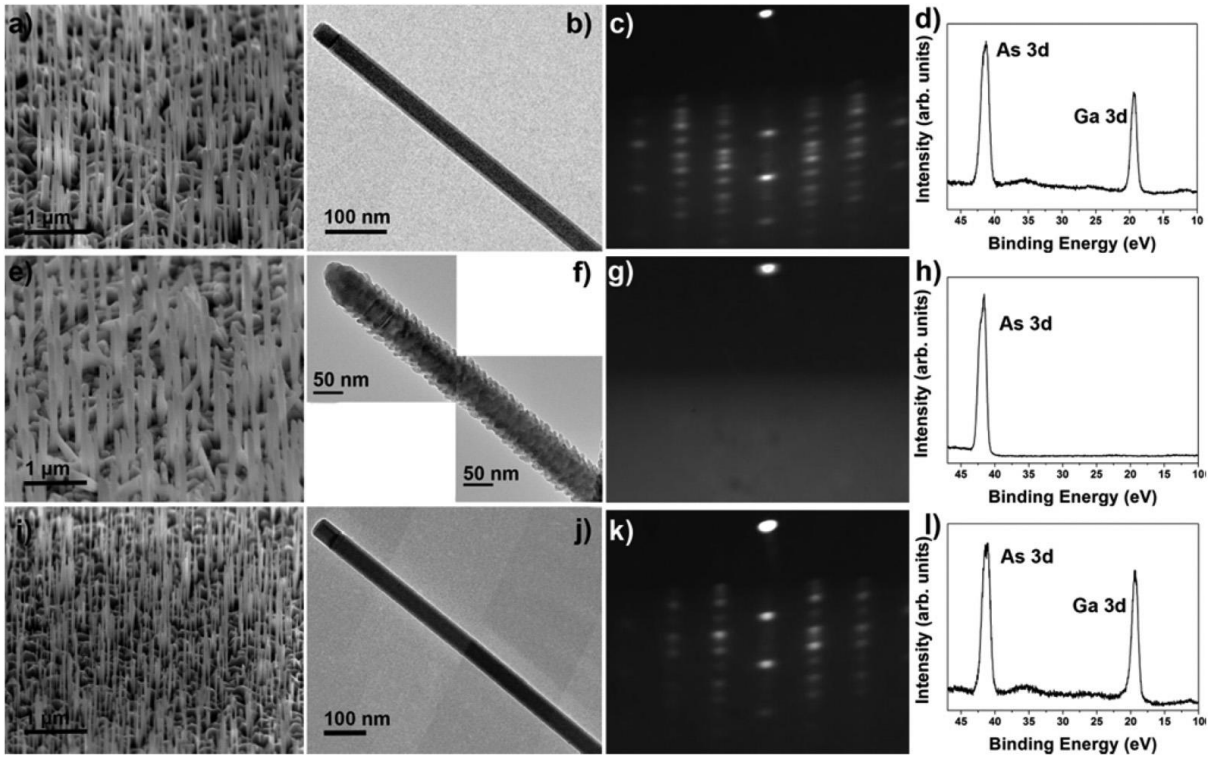

Figure 48. SEM image, TEM image, RHEED pattern along [110] and XPS spectrum of: a-d) as-grown GaAs NWs, e-h) NWs with As cap and i-l) NWs after As decapping under UHV.

To testify whether the oxidation-proof procedure is necessary and efficient, the reversible As-cap method was implemented right after the growth of GaAs NWs. Then, the capped sample was taken out of the MBE chamber and stored in the ambient air at RT for 24h without any other chemical or physical treatment, and finally reintroduced into the MBE chamber to remove the As layer via the soft thermal treatment. Afterwards, the decapped sample was transferred to the XPS chamber under UHV. XPS spectra of the decapped NW sample, displayed in Figure 47 row IV, are very similar to those of the as-grown GaAs NWs (Figure 47 row I). Neither As nor Ga oxides are detected, notably different from the results shown in Figure 47 row II and III. O 1s peak is also symmetrical, because of the only contribution origin from the native SiO_x which presents on the Si substrate. Similarly, the time-dependence was investigated. The air-exposure time was extended to as long as 2 months and other procedures were kept as the same. Only a little amount of Ga oxides is detected (Figure 47 row V), less than the quantity detected in Figure 47 row II. The efficiency of this oxidation-proof As capping / decapping method is well proved. However, it should be noted that this As-cap method is not competent enough for samples with a long time air-exposition. The relatively no-compact structure of amorphous As might offer the path for contaminations. The desorption of As also can cause the surface oxidation and contamination during long-time exposition. The time dependence of this reversible method will be necessary to be investigated.

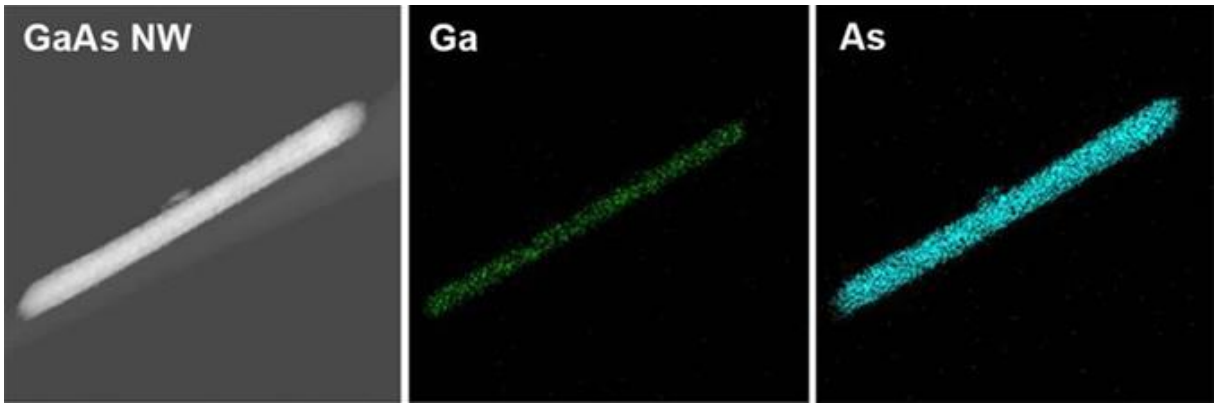

Figure 49. STEM image and EDX elemental mapping of an As-capped GaAs NW.

4. The impact on GaAs (core) / AlGaAs (shell) NWs

4.1. The impact on the structure of the AlGaAs shell

To further demonstrate the efficiency of the reversible As-capping / decapping method for the growth of an epitaxial shell, we investigated the growth of an AlGaAs shell on different GaAs NW samples. The first one corresponds to an as-grown GaAs NW array without exposure to ambient air, the second one is a GaAs NW array stored in ambient air at RT for 45 days and the third one is an As-capped GaAs NW array stored in ambient air at RT for 40 days and then decapped under UHV. The AlGaAs shell can passivate the surface of GaAs core for possessing a wider band gap than that of GaAs. Thanks to this AlGaAs layer, the PL measurements could be used to study the optical properties of these core / shell NWs and finally the quality of the core / shell interface (section 4.2).

For the first NW array, following the typical growth of the GaAs NWs in the MBE chamber, an AlGaAs shell was grown on the surface of the GaAs core right after the sample cooled from 610 °C to 515 °C under As_4 flux. This sample will be referred as "*in-situ* grown GaAs / AlGaAs NWs". The As_4 crystallized the Ga catalyst droplet on the tip of the NWs, inhibiting the axial growth to realize the radial growth after. TEM images (Figure 50 a) reveal the conformal growth of the AlGaAs shell on the GaAs NW facets. The HRTEM picture (Figure 50 b) clearly shows the continuous uniform lattice fringes of the shell material. The interplanar spacing is equal to 3.23 Å, attributed to the (111) planes of AlGaAs alloys. No interfacial layer between these two materials is observed. Through FFT analysis of the selected area around GaAs / AlGaAs interface, only one set of patterns is obtained, indicating that AlGaAs shell was epitaxially grown around the GaAs core.

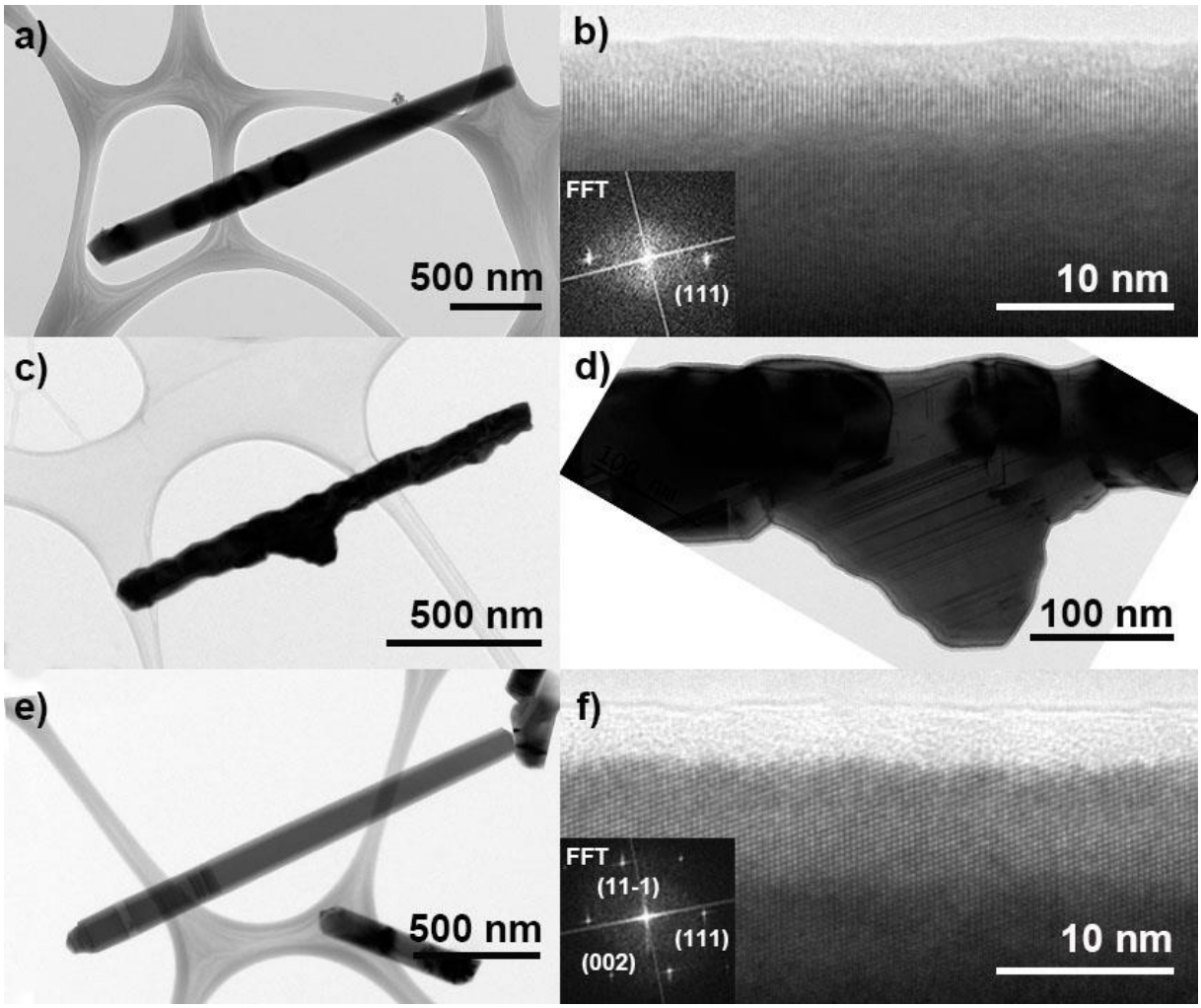

Figure 50. TEM and HRTEM images of a-b) an *in-situ* grown GaAs / AlGaAs NW, c-d) an oxidized-GaAs / AlGaAs NW and e-f) an As-capped-oxidized-decapped-GaAs / AlGaAs NW.

Apparently, in the case of the oxidized GaAs NW array, the newly formed surface of core / shell NWs is quite rough (Figure 50 c). From the TEM picture in higher magnification (Figure 50 d), abundant crystal defects are well observed in the entire shell in accordance with a polycrystalline growth of the AlGaAs shell and in turn the detrimental effect of the oxide interface layer on the morphology of NWs. This kind of structural disorder is clearly detrimental to the properties of the nanostructures.[26] Finally, for the third one, the As capped GaAs NW array, it was preserved under the ambient atmosphere for 40 days and then introduced back into the MBE chamber to remove the oxidation-proof As-cap under UHV, and to subsequently construct the core / shell NWs using the same procedure. As seen in Figure 50 e, NWs with smooth facets are also acquired. The HRTEM image and its corresponding FFT pattern (Figure 50 f) demonstrate the epitaxial growth, comparable to the results obtained from the *in-situ* grown GaAs / AlGaAs NWs. It should be noted that oxidized-GaAs NWs are also heated from RT to 440 °C in order to maintain a same heating history with the decapped ones. Figure 51 is the STEM image of a typical *in-situ* grown GaAs / AlGaAs NW and the corresponding EDX elemental mapping of Ga, As and Al elements. Ga

and As atoms disperse in both the core and the shell parts, while Al exists only in the shell (the intensity of the inner part is low).

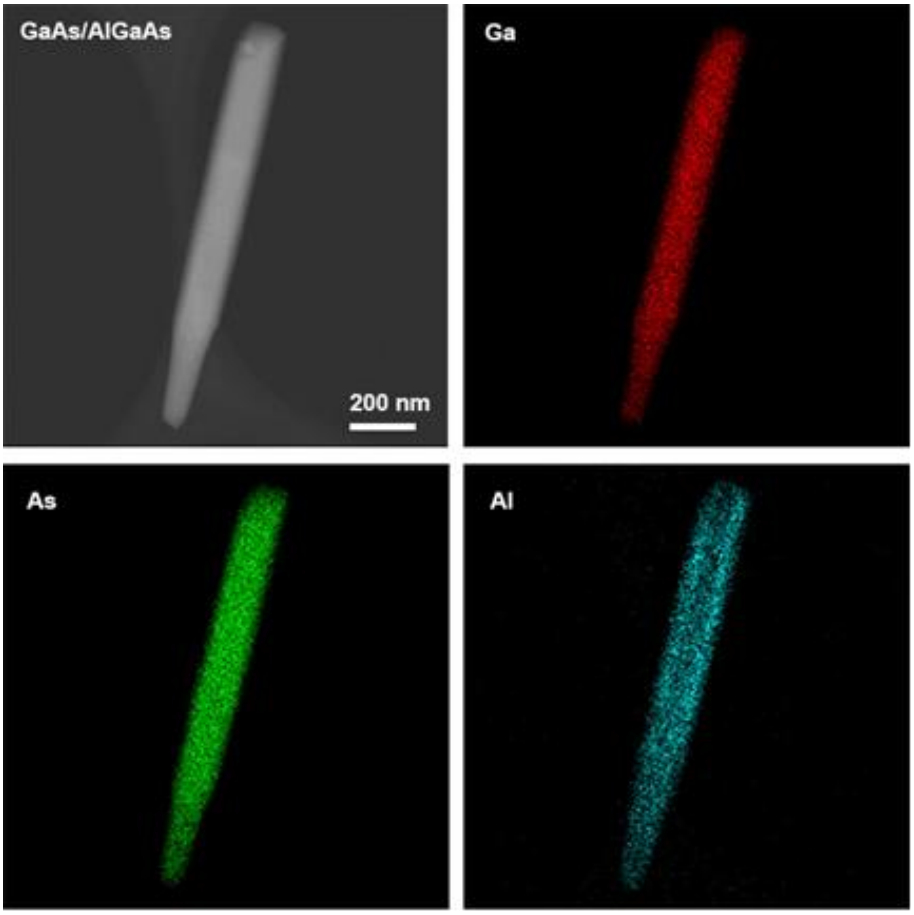

Figure 51. STEM image and EDX elemental mapping of one *in-situ* grown GaAs / AlGaAs NW.

4.2. The impact on the optical properties of GaAs / AlGaAs NWs

Except the effect on the structure of core / shell NWs, it is also very important to survey whether the uncontrolled oxidation and the As capping / decapping method show further impact on optical properties of NWs. Hence, Photoluminescence (PL) measurements were carried out for the comparison between the *in-situ* grown GaAs / AlGaAs NWs, the As-capped-decapped GaAs / AlGaAs NWs and oxidized-GaAs / AlGaAs NWs (in collaboration with N. Chauvin INL-INSA). Moreover, compared to TEM measurements, PL measurements provide a complementary characterization of the core / shell interface because of its sensibility to trapped carriers. The excitation power was provided by a 532 nm continuous wave diode-pumped solid-state laser (50 mW) and the detection by a nitrogen cooled silicon CCD detector coupled to a monochromator. Low temperature measurements were achieved by inserting the investigated samples in a closed-cycle helium cryostat.

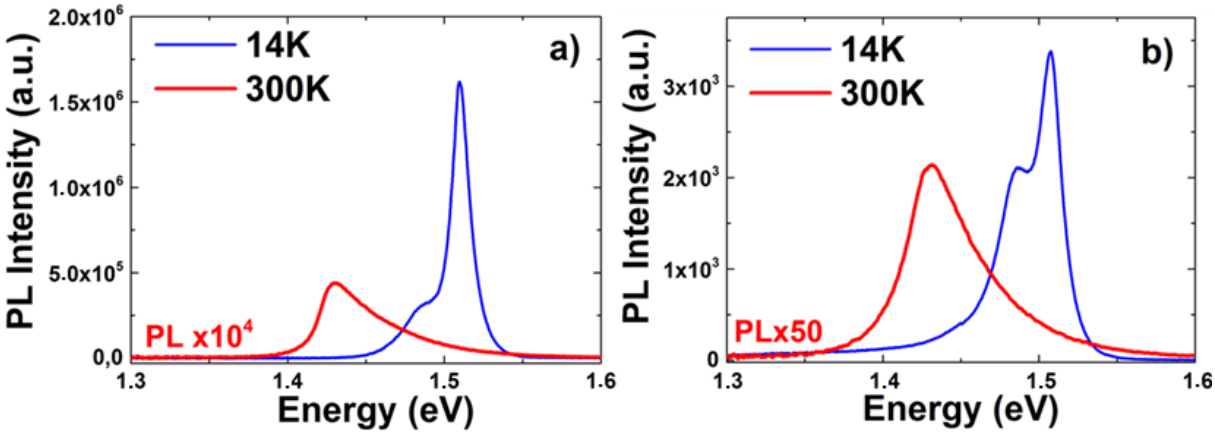

Figure 52. PL spectra of (a) the *in-situ* grown GaAs / AlGaAs NW and (b) As-capped-decapped GaAs / AlGaAs NWs registered at 14 K and 300 K.

As expected, the oxidized one didn't show any light emission due to the serious degradation of the shell structure and the poor core / shell interface quality. Herein, only the PL spectra of the two former samples are shown in Figure 52. At 300 K, the peaks are centred at around 1.43 eV, which is in agreement with the emission energy of GaAs NWs in ZB phase.[27,28] The PL intensity of both samples is comparable. At low temperature, 14 K, a sharp peak emitting around 1.509 eV and a much less intense shoulder in the 1.48-1.49 eV range are observed on both spectra. Nevertheless, the PL intensity of As-capped-decapped GaAs / AlGaAs NWs is 3 orders lower than that of the *in-situ* grown GaAs / AlGaAs NWs. If the sharp peak can be related to the exciton emission from ZB GaAs, the origin of the low energy shoulder has to be understood.

It should be reminded that, as aforementioned in Chapter 3, the HRTEM analysis reveals that WZ insertions are presented in the ZB NWs. It is known that ZB and WZ GaAs have an equivalent band gap at low temperature, while an energy spacing of 20 meV between the two crystallographic phases has been testified at RT.[27,29] The band alignment of WZ and ZB GaAs at low temperature is illustrated in Figure 53.[30]

As far as the *in-situ* grown GaAs / AlGaAs NWs are concerned, the PL intensity is also recorded as a function of the excitation power. Small blue-shifts of PL are detected when the excitation power is increased. This power-dependent behaviour is usually the signature of a spatial carrier separation in a type-II heterostructure in which electrons and holes are separated in adjacent different materials, thereby forming spatially indirect excitons.[31] Compared with that of a direct exciton in a type-I system where both electrons and holes are confined in the same layer, the wave-function of the indirect exciton is significantly extended in space, which largely enhances the controllability of the wave-function distribution (Figure 53). Besides, the relatively long radiative lifetime originating from the spatially indirect recombination is another characteristic of the type-II heterostructure, making them quite attractive for practical devices such as optical memories.[32,33] Concerning

the non-aligned band structure of ZB and WZ GaAs (Figure 53), this power-dependent emission in the range of 1.48-1.49 eV at 14 K could be attributed to the type-II recombination in ZB / WZ GaAs NWs: electrons located in the ZB phase combine with holes in the WZ insertions.[30,34,35] This assumption was then confirmed by the following time-resolved PL measurements.

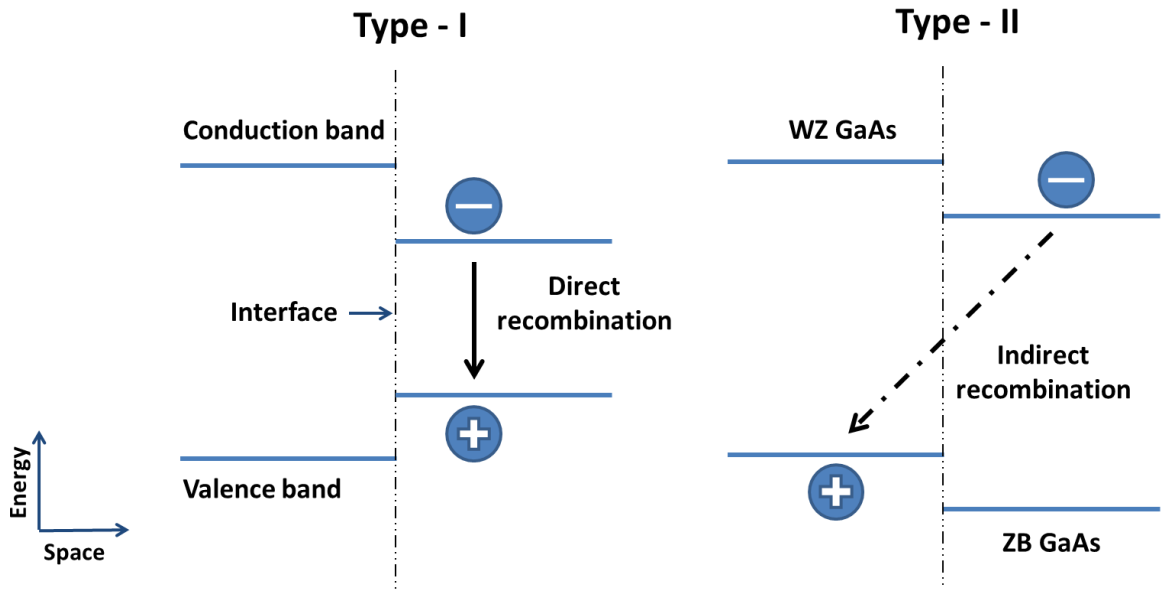

Figure 53. Schematics of the band structure in type-I and type-II heterostructures and their corresponding recombination processes. WZ / ZB GaAs heterostructure at low temperature serves as an example of the type-II one. The interface of the heterostructure is indicated by a black dashed line.

Time-resolved PL spectroscopy was performed at 14 K on both the *in-situ* grown and the decapped samples. Figure 54 a shows the PL decay of the *in-situ* grown sample for a lower excitation density (pulse excitation density of 24 nJ/cm²). The PL decay (Figure 54 b) is obtained by integrating the emission over a 4 nm window around the low energy peak. The exciton lifetime is extracted by using a mono-exponential decay:[36]

$$I_t = I_0 \exp(-t/\tau)$$

where I_o is the PL intensity at time *zero*, I_t is that at time *t*, and τ is the exciton lifetime. A relatively long exciton lifetime, 4.6 ns, is deduced in the case of the *in-situ* grown GaAs / AlGaAs NW array (Figure 54 b). This result confirms that the low energy shoulder has to be associated to a type-II WZ / ZB GaAs heterostructure.

The result is different from what is obtained from the As-capped-decapped GaAs / AlGaAs NW sample. First, no energy shift is observed on the low energy peak when the excitation power is modified. Moreover, a short decay time of 380 ps (Figure 54 c, d) is extracted from the data using the equation:

$$I_t = I_0 \exp\left(-\frac{t}{\tau}\right) + y_0$$

Thus, the low energy shoulder of the decapped sample is probably an impurity or a defect related emission. As this excitation-power-independent peak wasn't been observed for the *in-situ* grown GaAs / AlGaAs NWs, the impurities or defects are supposed locating at the interface of GaAs / AlGaAs heterostructure. A peak associated to the type II WZ / ZB heterostructure is probably present in the PL spectrum but is hidden by this new defect related emission.

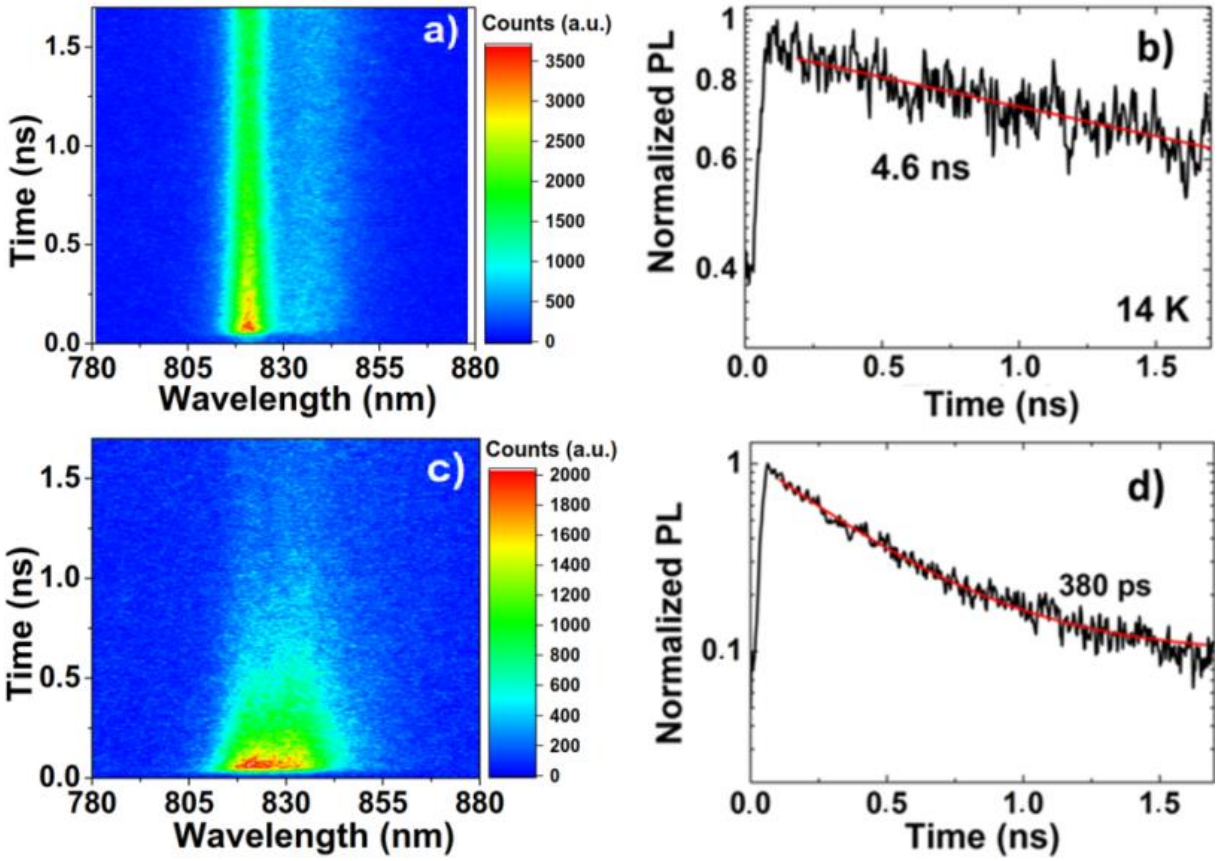

Figure 54. The PL intensity map of a) the *in-situ* grown GaAs / AlGaAs NW array and of c) the As-capped-decapped GaAs / AlGaAs NW array as a function of time and wavelength of the emitting light; b) and d) the corresponding decay times for the low energy peak. Measured at 14 K. Red lines in b) and d) represent fits to experimental data using mono-exponential decays.

As mentioned before, the low temperature PL emission of the decapped sample is 3 orders of magnitude weaker than *in-situ* grown GaAs / AlGaAs NWs (Figure 52). This is a clear indication that the As-capping-decapping process has induced non radiative centers at the GaAs / AlGaAs interface. As we discussed above, both samples present a similar PL emission intensity at 300 K. This means that during the heating procedure from 14 to 300 K in the PL chamber, other non-radiative processes present in both samples were thermally activated and turn to be dominating. Comparing to the effect of this thermo-activated non-

radiative channel, the non-radiative centers around the GaAs / AlGaAs interface for the decapped sample are less visible. Figure 55 shows the evolution of the integrated PL intensity for the two samples as a function of temperature (excitation provided by a 50 mW - 532 nm cw laser). The integration is performed over all the PL spectra including the low energy contribution. From 14 K to 300 K, the integrated PL emission is devided by 15,000 and 50 for the *in-situ* grown and the decapped samples, respectively. These results mean that the As-capping-decapping procedure is compatible with NW opto-electronic devices working at room or higher temperature.

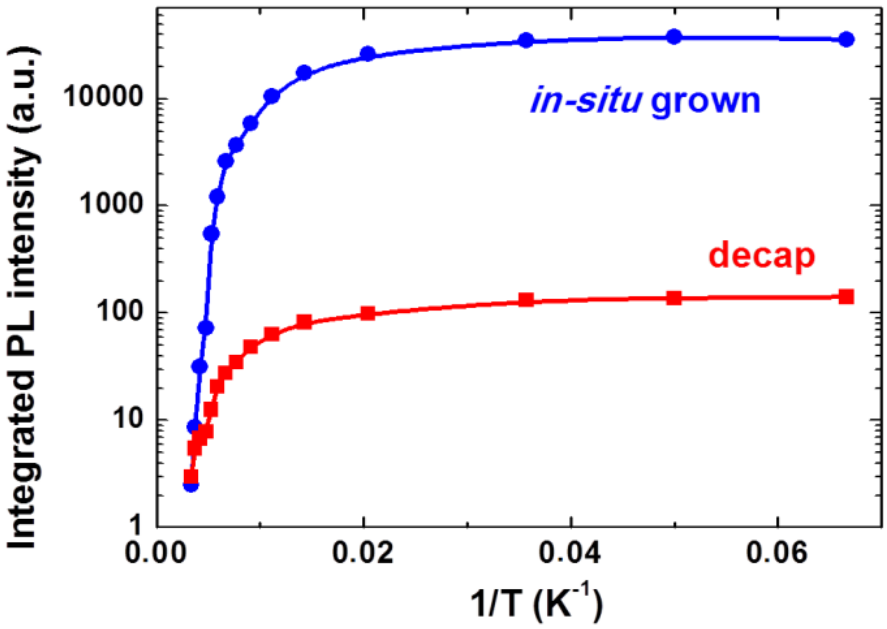

Figure 55. The integrated PL intensity as a function of the temperature for the *in-situ* grown GaAs / AlGaAs NW array (blue) and the As-capped-decapped-GaAs / AlGaAs NW array (red).

To quantify the quality of the GaAs / AlGaAs interface, decay times of the *in-situ* grown and the decapped samples are also measured for the GaAs band gap related peak. The decay times at 14 K are obtained by integrating the PL intensity around the high energy peak. A quite narrow wavelength window (4 nm) was set for the integration to discard all the contributions originating from the low energy shoulder. Whilst, the decay times at 300 K were obtained by the integration of all the emissions of NW arrays. The exciton lifetimes, at 14 K, are 710 and 320 ps for the *in-situ* grown and the decapped samples, respectively (Figure 56 a). While at 300 K (Figure 56 b), they are 94 ps and 80 ps, respectively.

The decay rate of one NW can be described by contributions from the bulk as well as the surface due to the surface recombination velocity (SRV). The NW decay rate γ_{NW} can be estimated by the following equation:[37]

$$\gamma_{NW} = \gamma_{Bulk} + \frac{4S}{d}$$

where d is the NW diameter and S is the SRV. In the present study, the SRV is related to the GaAs / AlGaAs interface. Supposing that the bulk contribution as well as the NW diameter counterpart is identical for both samples, the decrease of lifetime observed from the decapped sample is a consequence of a bigger SRV. This SRV increase, ΔS, is given by the relation:

$$\Delta S = \frac{d}{4}\left(\gamma_{decap} - \gamma_{Ref}\right)$$

Given a NW diameter of 50 nm, ΔS is equal to 2100 cm/s at 14 K and 2300 cm/s at 300 K, respectively. Moreover, the decay at low temperature provides a maximum boundary on the SRVs. It can be concluded that the SRVs are smaller than 1800 cm/s and 3900 cm/s for the *in-situ* grown and the decapped samples, respectively. It is well known that the SRV of unpassivated GaAs surfaces of NWs is very high: in the order of 10^5 to 10^6 cm/s.[38,39] As far as the GaAs / AlGaAs core / shell NWs are concerned, the SRV values in the 10^3 - 10^4 cm/s range have been reported.[40,41] Other studies have also observed long lifetimes of the order of 1 to 2.5 ns, however without providing any SRV value.[28,42]

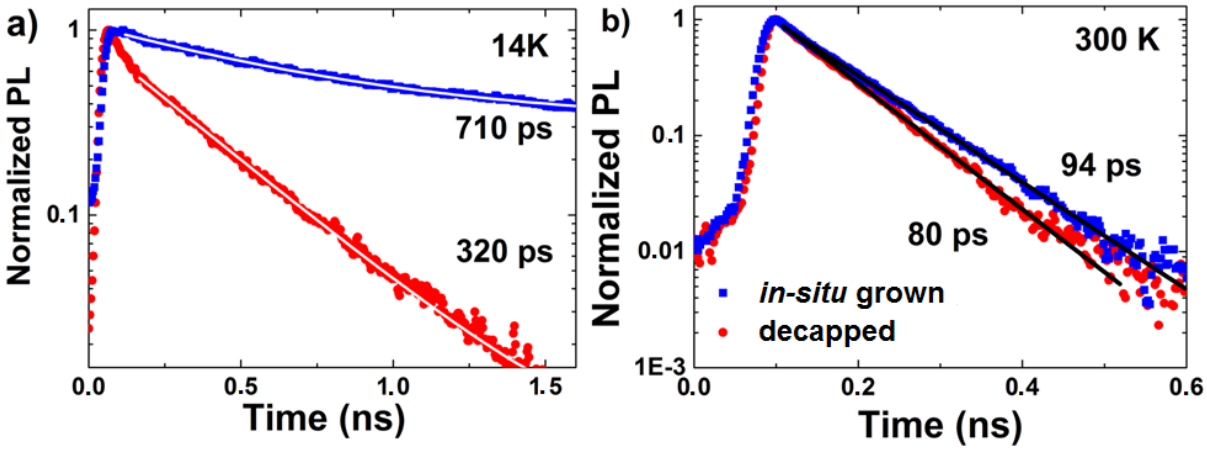

Figure 56. Time-resolved PL for the *in-situ* grown GaAs / AlGaAs NW array and the As-capped-decapped GaAs / AlGaAs NW array at a) 14 K and b) 300 K. Solid lines represent fits to experimental data by using mono-exponential decays.

5. Conclusion

In this chapter, optimized self-catalyzed GaAs NWs are used to study the surface oxidation effect. A simple and reversible As-capping-decapping method was also proposed in order to protect the active surface of GaAs NW core from uncontrolled oxidation and to realize an epitaxial core / shell heterostructure with better physical properties. Both elemental and crystal structural analyses proved the fatal effect of the uncontrollable NW

surface oxidation on the morphology, structural and optical properties of core / shell heterostructured NWs. This highly operable As-capping-decapping method opens the way to the integration of functional oxides, heterogeneous semiconductors and metals with III-V semiconductor NWs. Multifunctional devices coupling the outstanding properties of both core and shell materials might also be accomplished in the coming future.

6. References

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Chapter 5. Growth of GaAs (core) / functional-oxide (shell) NWs

1. Introduction

In the past two decades, core / shell NW heterostructures have attracted much attention in the research community. On one hand, the carrier confinement effect as well as their high specific surface area could enhance physical properties of the system and even generate new promising features.[1,2] On the other hand, the core / shell NW heterostructures offer the possibility to couple the physical properties from the core and the shell.[3-5] Although most of the published works on semiconductor-core / semiconductor-shell NWs concern semiconductors of the same family, the integration of heterogeneous materials such as silicon,[6,7] silicide[8] or metals[9] on GaAs NWs has been recently achieved opening the way to the fabrication of original devices. Functional oxides with perovskite structure are a very promising shell material. Firstly, it is theoretically possible to epitaxially grow this kind of materials on semiconductors like Si and GaAs with a small lattice mismatch.[10-12] Moreover, as known, perovskite oxides have notably similar crystallographic structures and thus stacking different ones layer by layer is rather operational. In this context, we propose a general method to construct semiconductor (core) / perovskite-oxide (shell) heterostructures and in turn to synthesis multishell NWs. Secondly, perovskite oxides possess a wide range of properties, such as piezo-electricity, ferro-electricity etc., which are complementary to those of semiconductors. This combination can facilitate the development of multifunctional devices. Thirdly, perovskite oxide NWs are difficult to prepare by the VLS method despite recent promising results.[13,14] The growth of semiconductor (core) / perovskite oxide (shell) NWs could be an alternative means to fabricate 1D functional oxide nanostructures.

Although this heterogeneous combination is obviously promising, achieving an epitaxial semiconductor / perovskite oxide heterostructures is challenging due to the rapid oxidation of classical semiconductors such as Si or III-V when exposed to air or O_2.[15,16] To prevent such phenomenon, R. Mc Kee *et al.* developed a strategy to passivate the Si substrate surface with half a monolayer of Sr that allows the growth of $SrTiO_3$ thin films directly on Si (001) by molecular beam epitaxy (MBE).[17] Such interface engineering has attracted considerable attention due to the possibility to grow functional oxides such as $BaTiO_3$,[18] $Pb(Zr_x,Ti_{1-x})O_3$[19] PMN-PT[20] on Si substrates. More recently, $SrTiO_3$ was successfully grown on GaAs substrates,[21-27] which is promising for the development of heterostructures coupling light emission / absorption and piezoelectricity or ferroelectricity.[28,29] Via a similar way, the fabrication of $SrTiO_3$ layers on the facets of GaAs NWs could open the way to the integration

of functional oxides on semiconducting NWs as a general strategy for all the perovskites oxides as we discussed before.

Hence in this chapter, we studied the growth of a $SrTiO_3$ shell on self-catalyzed GaAs NWs grown by VLS assisted MBE on Si(111) substrates. To better control the nucleation and growth of the $SrTiO_3$ shell, the GaAs NWs were protected via an As capping / decapping procedure in order to prevent uncontrolled oxidation and / or contamination of the NW facets as discussed in Chapter 4. RHEED, SEM, TEM and XPS measurements were performed to determine the structural, morphological and chemical properties of this heterostructured NWs. Using adapted oxide growth conditions, it is shown that most of the perovskite $SrTiO_3$ shell structure appears to be oriented with respect to the GaAs lattice. These results are promising for achieving 1D epitaxial semiconductor (core) / functional oxide (shell) nanostructures.

2. GaAs / $SrTiO_3$ NWs

2.1. The growth of GaAs / $SrTiO_3$ NWs

Confirmed by the discussion in Chapter 4, the profound harm of the uncontrolled oxidation is revealed. Also, the reversible As cap method is proven effective and can be used as a general method for protecting NWs from oxidation and contamination. So this method is applied to the construction of heterogeneous core / shell NWs, GaAs / $SrTiO_3$ NWs, for ensuring a relatively clean and abrupt interface. The schematic in Figure 57 illustrates all the synthesis procedure of GaAs / $SrTiO_3$ NWs. The As capped GaAs NWs array was prepared through the process presented in Chapter 4. The decapping step (Figure 57 a, b) was implemented in a MBE reactor, equipped with effusion cells for strontium (Sr) and titanium (Ti), which is dedicated to the growth of functional oxides. O_2 injection was controlled in a differentially-pumped pre-chamber connected to the reactor. A butterfly valve is used to adjust the O_2 flow.

In order to avoid the formation of amorphous oxides on the GaAs NW lateral surface, the two-steps growth process is used as proposed by G. Niu *et al.* for growing $SrTiO_3$ films on Si substrates.[30] The first step (Figure 57 c, d) consisted in depositing an amorphous $SrTiO_3$ buffer layer (≈ 2.5 nm) at 350 °C under low O_2 partial pressure of $5x10^{-8}$ Torr in order to obtain a relatively sharp interface. The $SrTiO_3$ buffer layer grown at low temperature might preserve the GaAs / $SrTiO_3$ interface. Annealing at 550 °C under UHV for 15 min led to crystallization of this $SrTiO_3$ buffer layer (Figure 57 e, f). As the second step (Figure 57 g, h), further $SrTiO_3$ growth was performed at higher temperature (550 °C) under higher O_2 partial pressure ($1x10^{-7}$ Torr). For a typical sample, the second $SrTiO_3$ layer growth took 15 min (≈ 2.5 nm). The corresponding RHEED patterns along [1-10] can also be found in Figure 57. It should be noted that before the decapping process, no diffraction pattern was visible, in agreement with the presence of an amorphous As capping layer. At 350 °C a diffraction pattern became visible (Figure 57 b), which testifies the desorption of As. Several low

intensity spots (marked by arrows in Figure 57 b) may come from WZ insertions present in the twinned-ZB GaAs NWs as well as from the parasitic crystals. After $SrTiO_3$ deposition at low temperature, the RHEED pattern does not show any change except a brighter background, in agreement with a thin amorphous layer (Figure 57 d). Then, during the annealing at 550 °C, rings appeared due to the $SrTiO_3$ crystallization without preferential orientation (Figure 57 f). During the second step of $SrTiO_3$ growth at 550 °C, rings become more intense (Figure 57 h). All the rings observed in Figure 57 h are in agreement with bulk $SrTiO_3$.

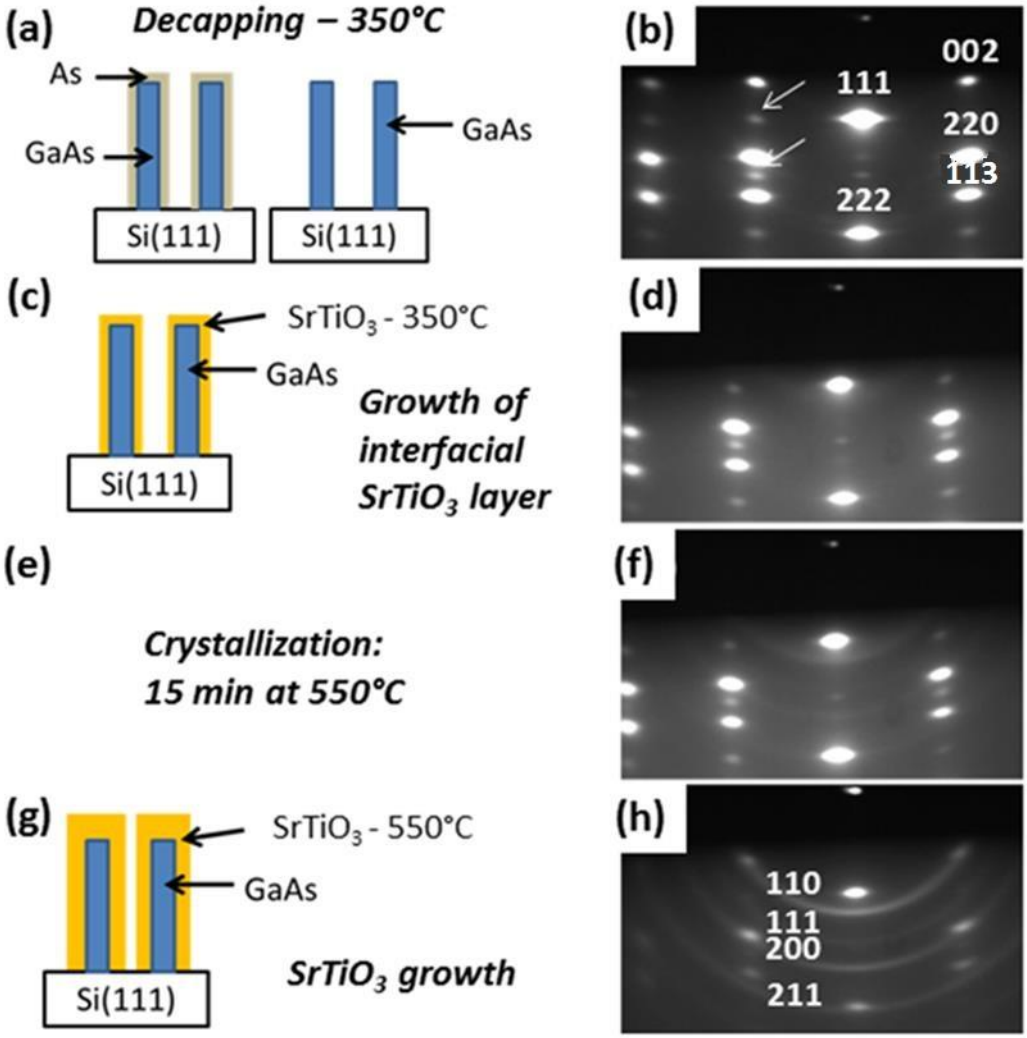

Figure 57. Illustration of the capping / decapping and of the two-steps $SrTiO_3$ growth processes a, c, e, g). RHEED pattern measured along the [1-10] azimuth: b) after the decapping of the As protective shell at 350 °C, d) after the growth of the $SrTiO_3$ buffer layer during 15 min at 350 °C, f) after the annealing during 15 min at 550 °C and h) after the growth of $SrTiO_3$ during 15 min at 550 °C.

2.2. Structure, morphology and chemistry of GaAs / $SrTiO_3$ NWs

2.2.1. GaAs / $SrTiO_3$ NWs grown by the one-step method

In order to investigate the impact of the growth temperature on structural and morphological properties of the $SrTiO_3$ shell, a series of sample was prepared by a one-step method for comparison with the two-steps one. The so-called one-step method is a deposition of 40 MLs of $SrTiO_3$ under a low O_2 partial pressure (5 x 10^{-8} Torr). Three different growth temperatures were investigated, 350, 450 and 620 °C, respectively.

Figure 58 shows TEM measurements performed on the sample with a $SrTiO_3$ shell grown at 350 °C. At the beginning of the growth, the RHEED pattern was consistent with GaAs NWs.

During the $SrTiO_3$ growth, the spot intensity decreased slowly in accordance with an amorphous layer covering the GaAs NWs as expected at such a low temperature and described in the former section. As shown by the low magnification TEM image (Figure 58 a), the newly fabricated surface of the core / shell NWs is rather smooth and the $SrTiO_3$ layer is quite uniform. However, in HRTEM images, besides amorphous layer (Figure 58 b), some crystallites of $SrTiO_3$ are also observed (Figure 58 c). Revealed by the FFT analysis (Figure 58 c insert) of the zone marked by a red square in Figure 58 c, the observed lattice is ascribed to $SrTiO_3$ (110). However, there is no particular epitaxial relationship between the $SrTiO_3$ shell and the GaAs core. Either the $SrTiO_3$ starts to be crystallized at such low temperature, or some parts of the shell are very sensitive to the electron beam during the TEM measurement. Finally, for confirming the core / shell heterostructure, EDX line scan (Figure 58 e) was performed, corresponding to the marked white line in the STEM image of one typical core / shell NW (Figure 58 d). Ga and As exist only in the core, while Sr and Ti are distributed in the shell. The asymmetry of distribution is also caused by the shadowing effect as aforementioned.

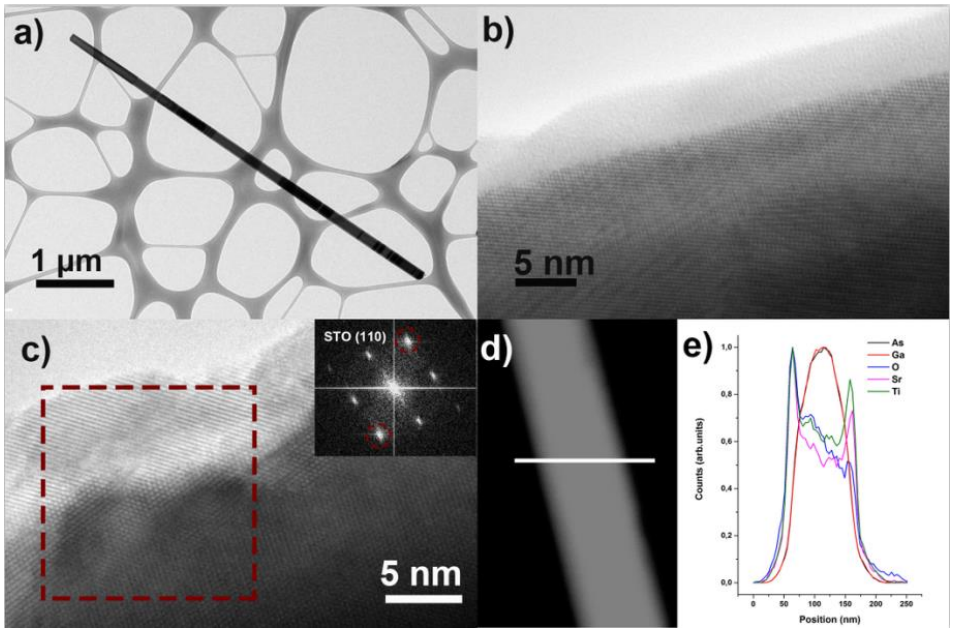

Figure 58. a-c) TEM images of GaAs / $SrTiO_3$ NWs with the $SrTiO_3$ shell grown at 350 °C. d) STEM image of a typical NW. e) EDX line scan corresponding to the marked white line in d).

The second NW array was obtained by growing the $SrTiO_3$ layer at 450 °C under the same oxygen partial pressure. As shown in TEM images (Figure 59 a), a lot of small particles are distributed on the NW surface, making it uneven, while some parts of the $SrTiO_3$ layer are still amorphous (Figure 59 b). However, the shell didn't shown hints of an epitaxial growth. Rings in accordance with polycrystalline $SrTiO_3$ are evidenced in the electron diffraction pattern (Figure 59 d) taken from the region displayed in Figure 59 c.

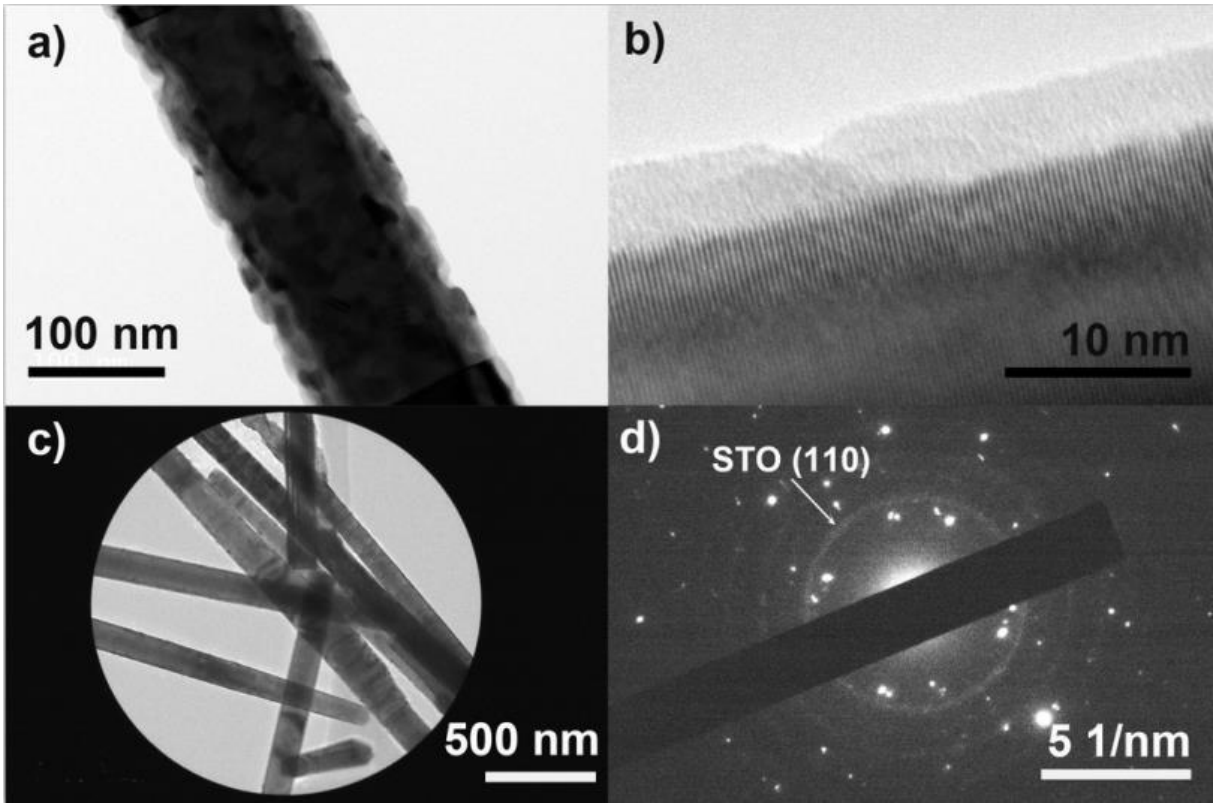

Figure 59. a-c) TEM images of GaAs / $SrTiO_3$ NWs with the $SrTiO_3$ shell grown at 450 °C, d) SAED pattern corresponding to the region shown in c).

The $SrTiO_3$ growth temperature was then increased to 620 °C for the last sample. As expected, the $SrTiO_3$ layer is well crystallized. Small pyramid-shaped $SrTiO_3$ crystals are formed at the surface of the GaAs NWs core, giving to the core / shell NW a faceted surface (Figure 60). A FFT process was performed for the marked zone in Figure 60 c. A typical cubic pattern was obtained with an interplanar spacing equal to 2.76 Å attributed to $SrTiO_3$ {110} planes (Figure 60 c). The relative orientation of this crystal and the GaAs NW core obtained directly from Figure 60 c is GaAs[111] // $SrTiO_3$[1-10]. Unfortunately, it is one special case, while the majority of $SrTiO_3$ crystals were grown randomly without a favourable orientation, such as the particle with the [110] blue arrow in Figure 60 c.

In summary, at low growth temperature (350 °C), $SrTiO_3$ was mainly amorphous while growing at high temperatures promoted the $SrTiO_3$ crystallization with some epitaxial crystallites that induces the formation of “dewetted” islands which also avoid the formation of a continuous shell that perfectly wraps the NWs core. The two-steps $SrTiO_3$ growth method allows obtaining a relatively good wetting due to the low deposition temperature for the first step as a buffer layer while the second step allows obtaining the $SrTiO_3$ perovskite crystalline structure.

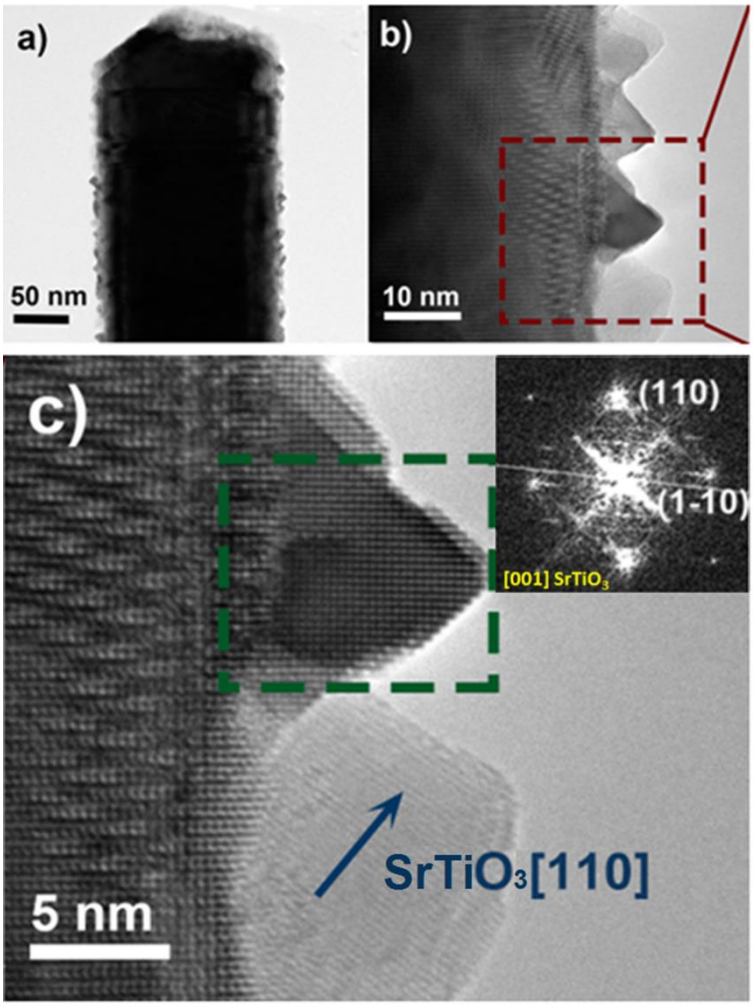

Figure 60. TEM images at different magnifications of the side surface of a typical GaAs / $SrTiO_3$ NW grown at 620 °C.

2.2.2. GaAs / $SrTiO_3$ NWs grown by the two-steps method

2.2.2.1. NW morphology and crystal structure

Comparing to NWs grown via the one-step method, the integration of GaAs and $SrTiO_3$ through the two-steps method is more desirable. The composition of the NWs was studied by EDX elemental mapping as shown in Figure 61 a, b. The results clearly show the presence of the $SrTiO_3$ shell wrapping the GaAs core. Figure 61 c shows the composition profile along the cross section of the NW. When compared to the rest of the NW, the tip exhibits an enrichment of $SrTiO_3$. This is probably the consequence of the configuration of the NW array and of the geometry of the MBE reactor that induced a preferential deposition on the tip rather than on the facets of the NWs.

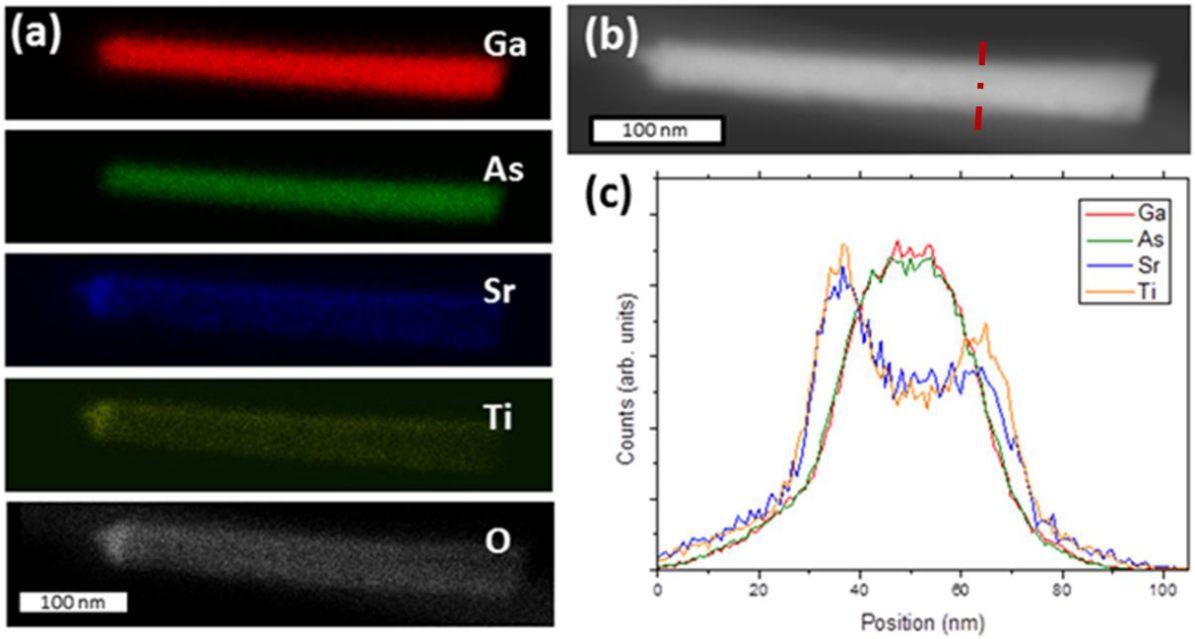

Figure 61. a) EDX mapping of Ga, As, Sr, Ti and O, respectively, for a single NW, b) its corresponding STEM image for a spot size of 1.5 nm, c) EDX line scan performed along the red dashed line marked in b).

To ensure the radial growth of $SrTiO_3$, EDX line scans were measured along the direction perpendicular to the NW growth direction for six more NWs. Sr, Ti and O elements were systematically detected. For most of the cases (Figure 62 b, c, e and f), the line scans are in accordance with a core / shell morphology, similar to Figure 61 c. However, in some cases (Figure 62 a, d), a distribution asymmetry of the Sr, Ti and / or O elements is detected. In Figure 62 d, an entire GaAs side is not covered by $SrTiO_3$ which could be the consequence of a shadowing effect which has been largely reported in the literature. The main causes of the shadowing are:

- The incident deposition flux is not perpendicular to the substrate surface;[31]
- NWs are not verticals, so some facets are not well exposed to the incident beam flux;
- Lengths of NWs are not uniform, so shorter NWs are shadowed by their longer neighbours;[32,33]
- The arrival of vapour atoms at the sidewalls may be restricted due to the high NW densities;[33,34]
- The incident beam flux is intercepted by the upper part of NWs, termed as base shadowing,[35,36] especially for NW arrays with long average lengths and high densities.

In order to avoid the self-shadowing effect, several parameters must be adjusted as the growth rate,[37] the incidence angle of the beam flux,[37] the substrate rotation speed,[37,38] the control of the NW density by lithography for a precisely spreading of catalytic droplets[39,40]

and the NWs verticality. In our case, the probable reasons for the shadowing effect could be that few NWs are not verticals and also, despite the low NW density, that some NWs appear to be very close from each other.

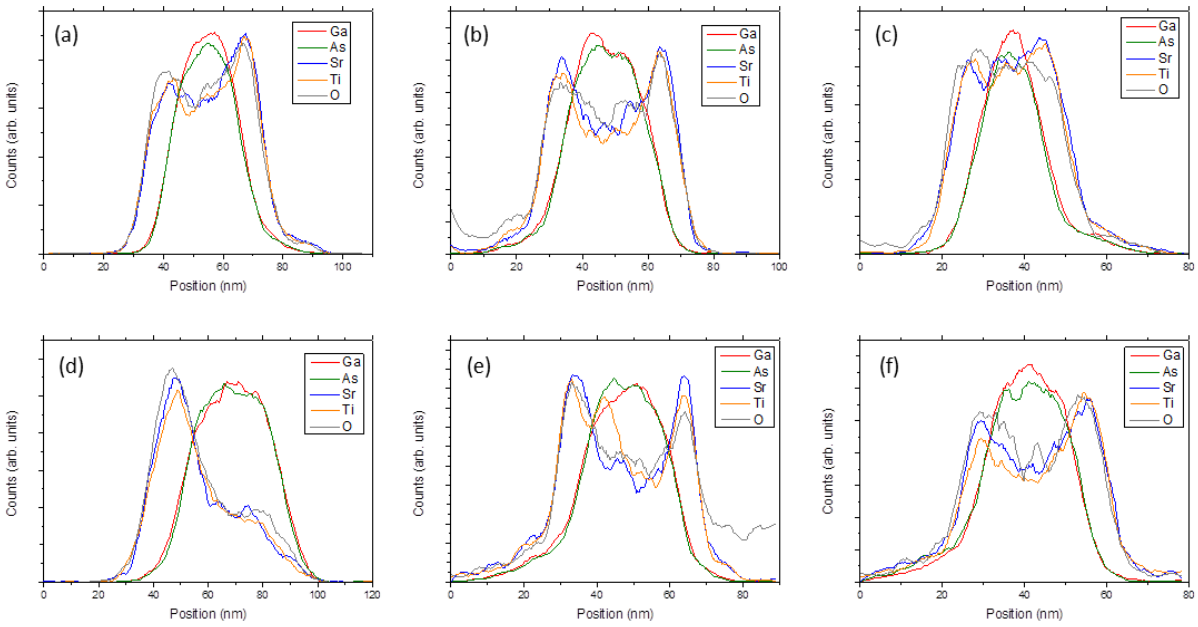

Figure 62. EDX line scan performed along six different GaAs / $SrTiO_3$ NWs.

Figure 63 shows TEM images of the GaAs NWs after the growth of the $SrTiO_3$ shell. The NW surface is relatively rough because $SrTiO_3$ seems to form agglomerated nanocrystals or faceted shell (Figure 63 c). The GaAs surface is well covered by $SrTiO_3$ even if some NWs exhibit regions free of $SrTiO_3$ (Figure 62 d) probably due to the shadowing effect during the oxide growth as discussed above. The quantity of $SrTiO_3$ deposited was equivalent to a 10 nm-thick layer. As the NW array is with a density of 7 NWs/µm², 45 nm in diameter and 1.0 µm in length, the specific area of the GaAs NW array (containing the surface between NWs) is one time bigger than that of a GaAs 2D layer of the same mass. Assuming the growth of a 2D $SrTiO_3$ layer on GaAs as reported,[29] the $SrTiO_3$ shell thickness should be about 5 nm, well in good accordance with the TEM image.

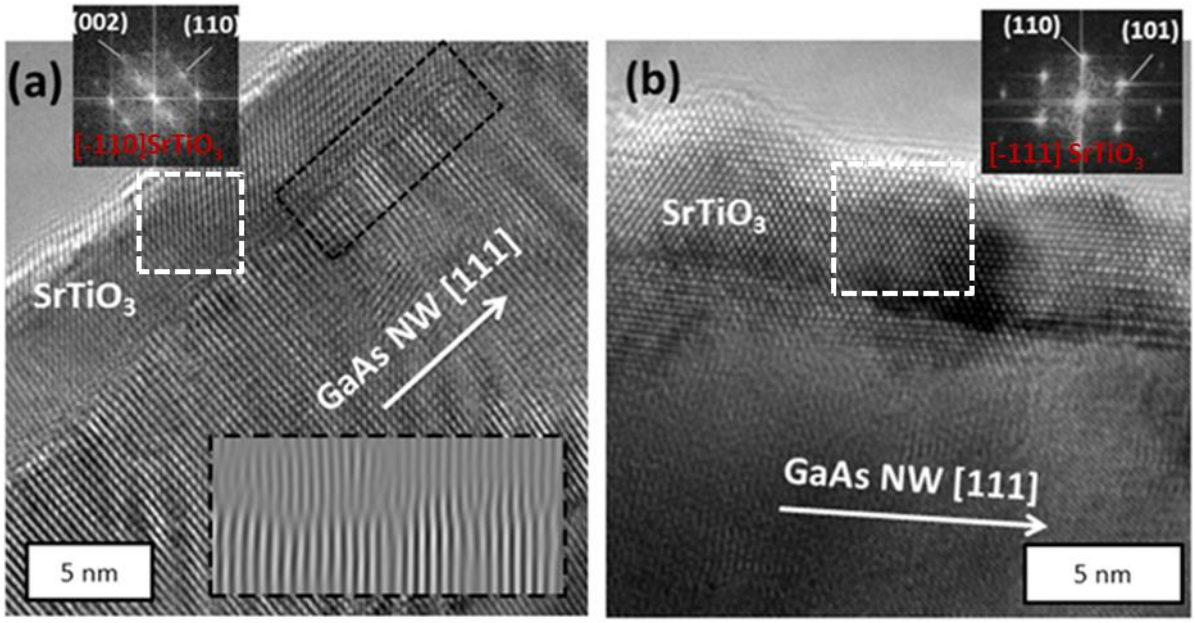

Figure 63. TEM images of an abrupt a) and an amorphous b) GaAs core / $SrTiO_3$ shell NW interface. FFT patterns are obtained from the selected regions marked by dashed white frames.

In Figure 63 a, some regions clearly exhibit Moiré fringes due to the overlapping of $SrTiO_3$ and GaAs lattices. The chemical composition of the shell measured by EDX mapping is in accordance with the $SrTiO_3$ stoichiometry. Most of the $SrTiO_3$ layer appears to be oriented with respect to the GaAs lattice. Measurements performed on the spots of the upper FFT in inset of Figure 63 a are in good agreement with the (002) and (110) reflections of $SrTiO_3$. The corresponding lattice spacing is 2.29 Å and 2.76 Å, respectively. The alignment of $SrTiO_3$ [110] with GaAs [111] results in a high mismatch that induces the formation of interfacial dislocations as shown in the filtered image of the interface (inset of Figure 63 a). The interface is abrupt but not perfectly flat, which could be the consequence of GaAs / $SrTiO_3$ interfacial reactions or of micro-faceting of the GaAs NW (note that {111} micro-facets have been already reported[41]).

Figure 63 b shows another interface between a $SrTiO_3$ layer and the GaAs NW core. Although the interface is not abrupt and seems to be partially amorphous, some parts of the $SrTiO_3$ layer are epitaxially grown on the GaAs lattice. The $SrTiO_3$ lattice is clearly identified, the FFT of the lattice shows three series of spots related to {110} planes. From this image, it can be deduced that the $SrTiO_3$ [1-12] is aligned with the NW growth direction which is GaAs [111]. If the GaAs NW facets are {1-10} planes, as reported,[42] $SrTiO_3$ [-111] would be aligned with GaAs [11-2]. Such alignment could minimize the mismatch to as small as 2.3% along $SrTiO_3$ [1-12] // GaAs [222] and $SrTiO_3$ [-111] // GaAs [11-2]. Another alignment, GaAs [1-10] // $SrTiO_3$ [110], can also be easily deduced. Figure 64 shows a possible model of the interface between $SrTiO_3$ layer and GaAs (1-10) facet in accordance with the lattice matching in Figure 63 b.

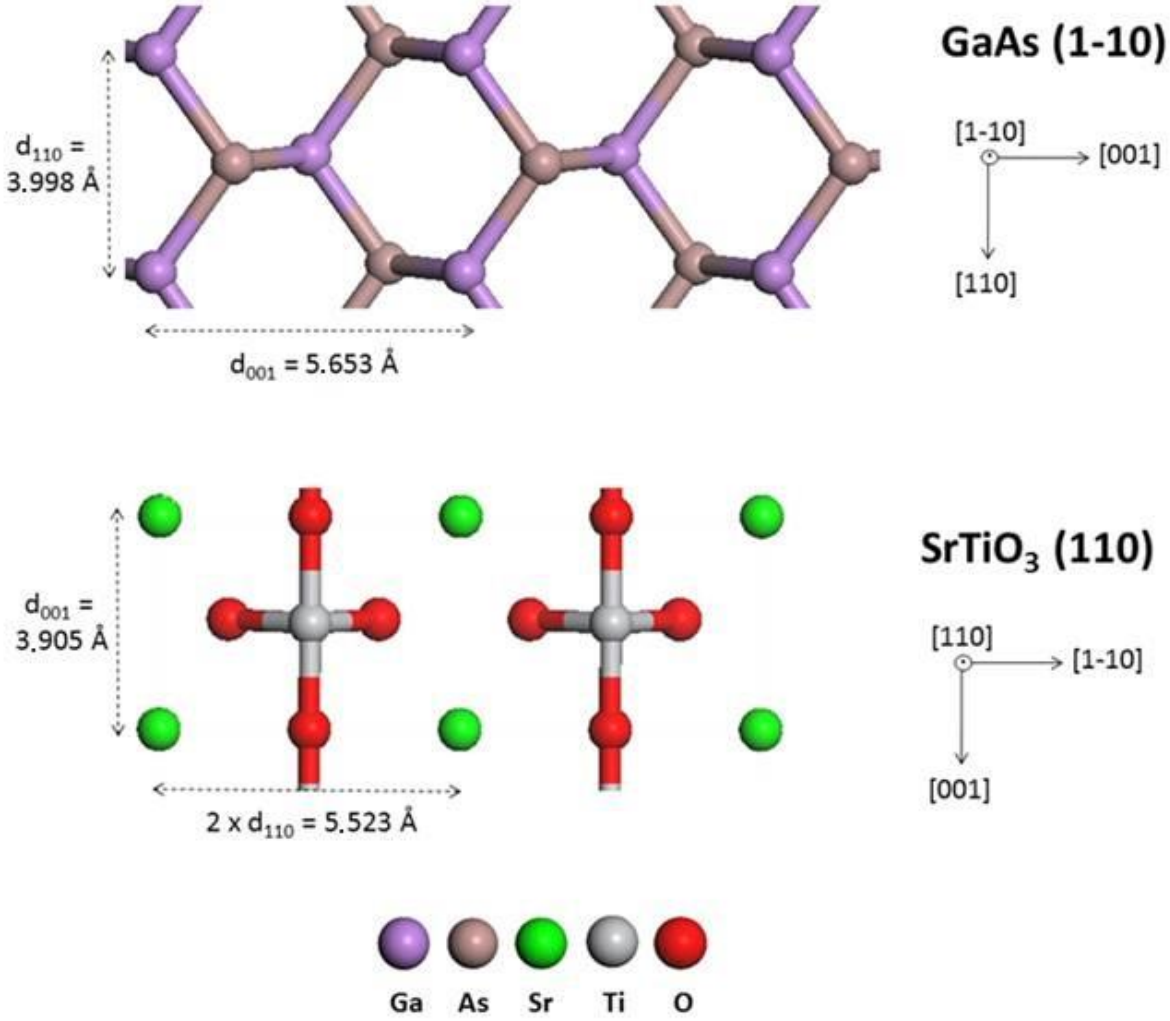

Figure 64. Ball and stick model showing the GaAs(1-10) plane and the $SrTiO_3$ (110) plane.

As shown in previous studies, the epitaxial growth of $SrTiO_3$ on Si(001) or GaAs(001) substrate is mainly driven by the minimization of the lattice mismatch leading to the alignment of $SrTiO_3$ [100] with Si [1-10][43-45] or with GaAs [1-10].[26,27] Unfortunately, others substrate orientations weren't intensively studied. J. Hao *et al.* reported on the growth of (110) oriented $SrTiO_3$ crystal on Si(001)[46] and also on Si(111) and Si(110)[47]. To our knowledge, there is no study reporting on the $SrTiO_3$ growth on GaAs(110) or (111) substrate.

Based on the work of G. Delhaye *et al.*,[43] we know that an amorphous interface can be formed after the oxide layer deposition on a semiconductor. In our case, an abrupt interface was found for several NWs as shown in Figure 65. It is also observed that some $SrTiO_3$ nanocrystals can agglomerate on the surface of GaAs NW core, particularly at the NW tip as displayed in Figure 66.

To summarize, both sharp and amorphous interface are evidenced in the as-grown GaAs / $SrTiO_3$ NW array using the two-steps growth method. Similar to the classical 2D growth, the amorphous interfacial layer can be formed after the $SrTiO_3$ growth which is compatible with an epitaxial growth under oxygen partial pressure. However, some NWs exhibit polycrystalline features, particularly around the tip of NWs.

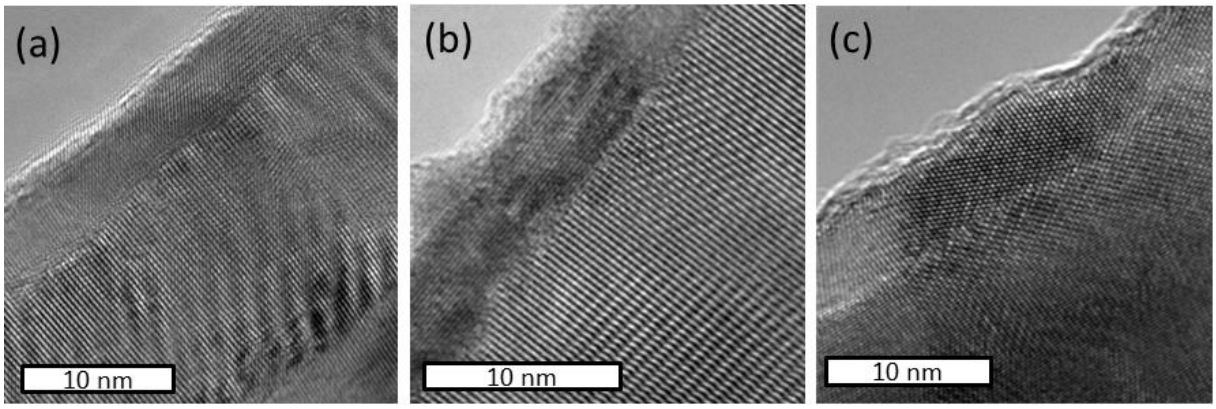

Figure 65. TEM images showing abrupt GaAs / $SrTiO_3$ interfaces. $SrTiO_3$ was grown using the two-steps method.

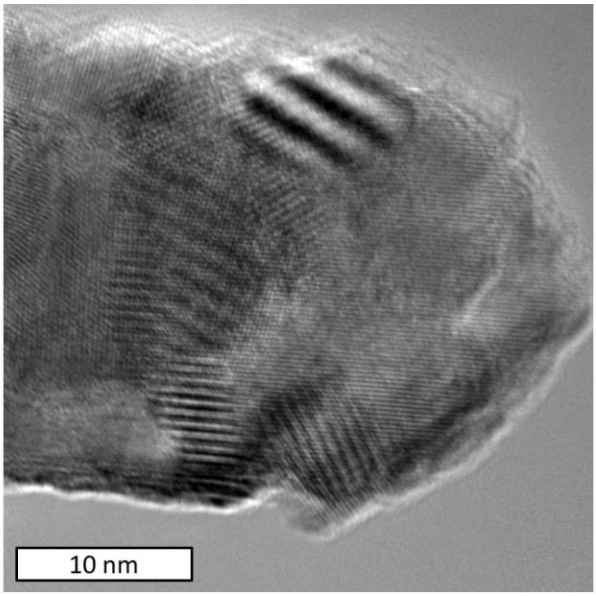

Figure 66. TEM image of a NW tip.

As known, there is a difference of polarity between different crystal plans. The most studied interface between GaAs and $SrTiO_3$ involves the polar GaAs (001) plan and the non-polar $SrTiO_3$ (001) plan.[10,21,48] In the GaAs / $SrTiO_3$ NWs, the GaAs {1-10} surface is non-polar while the $SrTiO_3$ {110} surface is polar. A more precise XPS analysis of $SrTiO_3$ on GaAs (110) substrate should be performed in order to understand how the $SrTiO_3$ bonds to the GaAs surface using the two-steps growth procedure.

2.2.2.2. XPS measurements

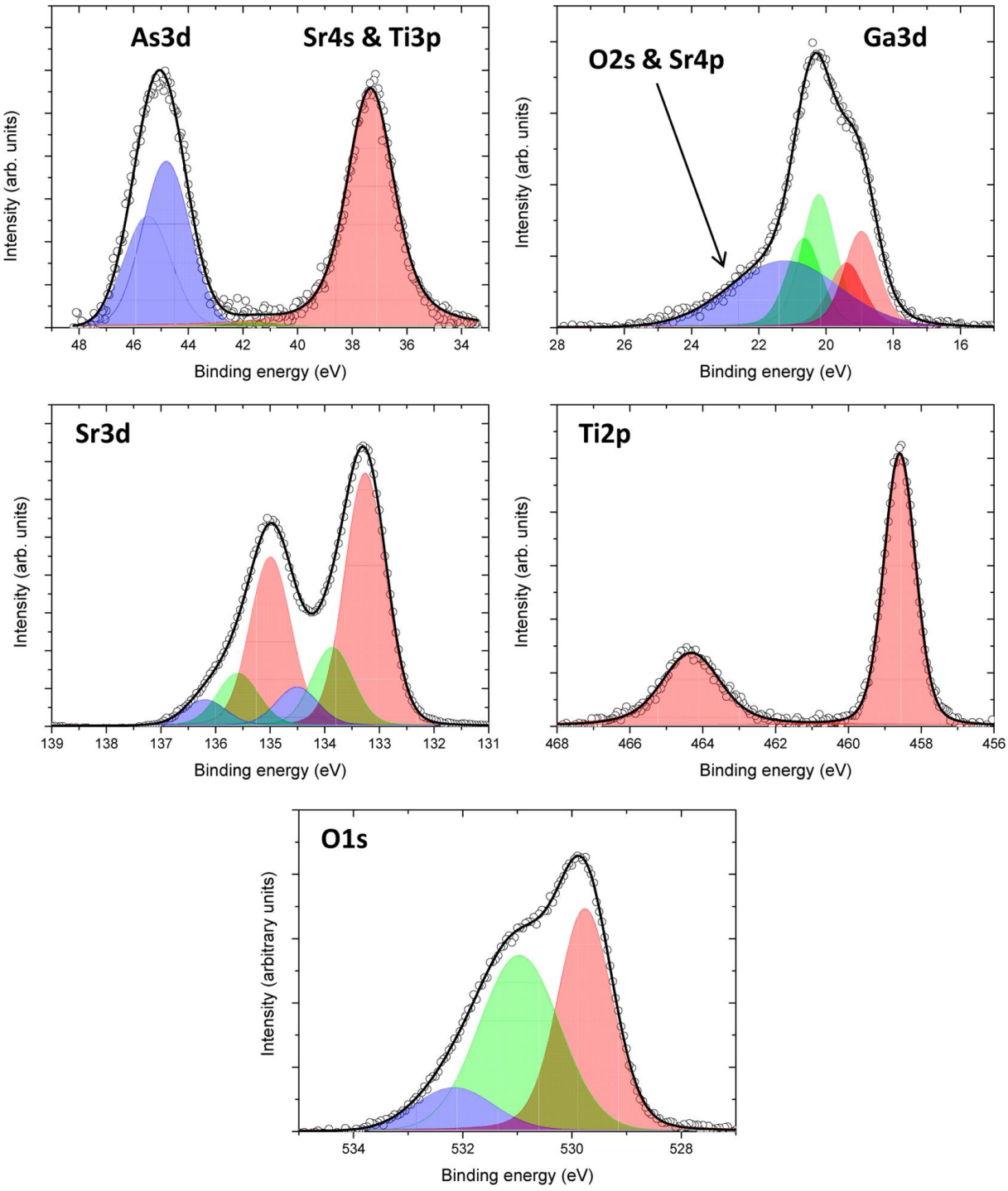

Figure 67. XPS core levels of GaAs / $SrTiO_3$ NWs measured at RT. The photon energy was 750 eV.

XPS measurements on GaAs / $SrTiO_3$ NWs were performed on TEMPO beamline at Soleil synchrotron facility, with a photon energy of 750 eV and a resolution of about 70 meV.[49] Figure 67 shows As 3d, Ga 3d, Sr 3d, Ti 2p and O 1s core levels before annealing. The Ti 2p core level is made of a single spin-orbit doublet (Ti^{4+}) with a spin-orbit splitting of 5.73

eV.[11,50,51] The Sr 3d core level exhibits a main spin-orbit doublet with Sr $3d_{5/2}$ at 133.2 eV and a spin-orbit splitting of 1.74 eV as in bulk $SrTiO_3$[50-52] and two other spin-orbit doublets at 133.8 eV and 134.5 eV for Sr $3d_{5/2}$. These latter peaks relates to the presence of stacking faults and SrO, respectively.[51,52] The formation of SrO in MBE-grown $SrTiO_3$ is attributed to the Sr segregation at the surface and at the interface during growth. The Ga 3d core level consists in a spin-orbit doublet corresponding to GaAs with Ga $3d_{5/2}$ at 18.9 eV and a spin-orbit splitting of 0.4 eV,[53] and in an intense component at 20.1 eV corresponding to Ga oxides. Contributions from O 2s and Sr 4p core levels are also reported. The As 3d peak position at 44.8 eV corresponds to As oxides, and not to the As 3d doublet (spin-orbit of 0.69 eV), which would appear around 41 eV between the Sr 4s / Ti 3p peak and As oxide peak. Therefore, an oxidized GaAs has been formed either at the GaAs NW surface after growth due to a partially inefficient passivation of GaAs NWs or at the GaAs / $SrTiO_3$ interface during $SrTiO_3$ growth. The core level O 1s also shows three components at 532.15, 530.94 and 529.74 eV attributed to $SrTiO_3$, As oxides and Ga oxides. The main XPS fitting parameters used in Figure 67 are summarized in Table 1. The fittings were achieved via Fityk 0.9.8.[54]

Table 1. Fitting parameters used for the peak decomposition of XPS spectra shown in Figure 67.

Core level	Binding energy (eV)	Spin orbit splitting (eV)	G-Width (eV)	Voigt parameter
Ti $2p_{3/2}$	458.59	5.73	0.55	0.19
Sr $3d_{5/2}$ A	133.24	1.74	0.51	0.08
Sr $3d_{5/2}$ B	133.84	1.74	0.51	0.08
Sr $3d_{5/2}$ C	134.49	1.74	0.51	0.08
Ga $3d_{5/2}$ A	18.91	0.45	0.65	0.19
Ga $3d_{5/2}$ B	20.18	0.45	0.65	0.19
As $3d_{5/2}$ A	44.78	0.69	1.22	0.00
As $3d_{5/2}$ B	41.57	0.69	1.22	0.00
O 1s A	529.74		0.63	0.17

O 1s B	530.94		1.04	0.00
O 1s C	532.15		1.00	0.00
O 2s & Sr4p	21.21		2.28	0.00

The thermal stability of the NW heterostructure was probed by measuring the Ga 3d, Ti 3p and As 3d core levels during annealing inside the XPS analysis chamber. Figure 68 shows the evolution of the XPS core levels during the annealing from room temperature up to 550 °C. The sample appears to be stable under UHV for temperatures below 500 °C. A slight decrease of the As 3d binding energy should be ascribed to the change of oxide composition caused by the annealing. At 500 °C, the As 3d intensity of As oxides abruptly decreases while a new component related to GaAs appears at around 41 eV. No significant evolution of the Ga oxide component is observed, which indicates a better stability of the Ga oxides compared to the As oxides.[55] The sample was then cooled down to RT and the Ga 3d, As 3d, Sr 3d and Ti 2p core levels were measured again. Interestingly, except for the As oxide desorption (O 1s and As 3d core levels) no other chemical modifications were observed, which can be recognized more easily from the comparison of XPS spectra obtained before and after annealing in Figure 69. Thus, XPS spectra of Ti 2p, Ti 3p, Sr 3d and Sr 4s core levels are almost identical before and after the thermal stability test. These results demonstrate the good thermal stability of GaAs / $SrTiO_3$ interface and the possibility to desorb the As oxide by a simple annealing. This thermal stability may also benefit the further growth of another functional oxide, such as the ferroelectric $BaTiO_3$, to construct the core / multishell NW array and the further practical devices.

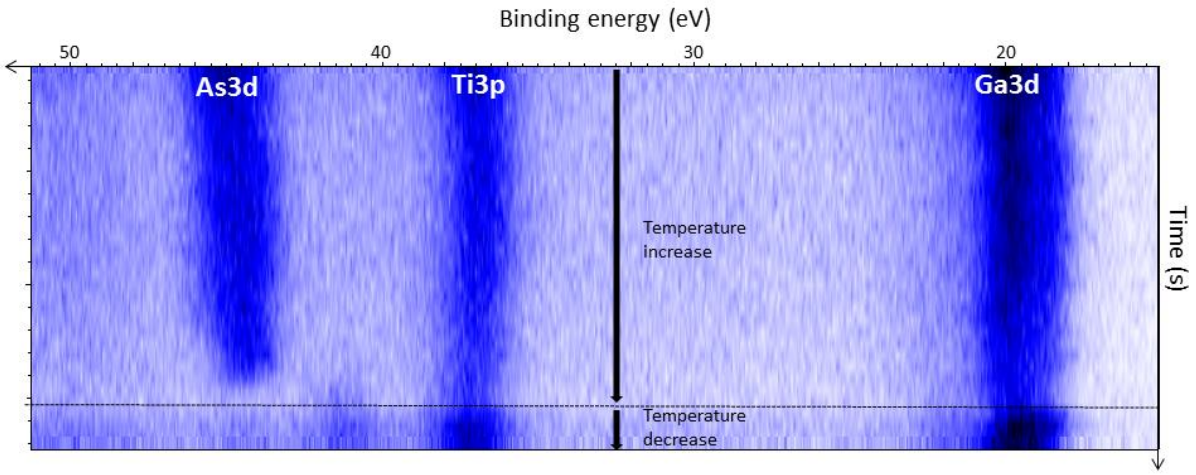

Figure 68. Evolution of the As 3d, Ti 3p and Ga 3d core levels of GaAs / $SrTiO_3$ NWs as a function of the temperature during annealing from RT to 550 °C and cooling. The maximum temperature corresponds to the dashed line. The photon energy was 750 eV.

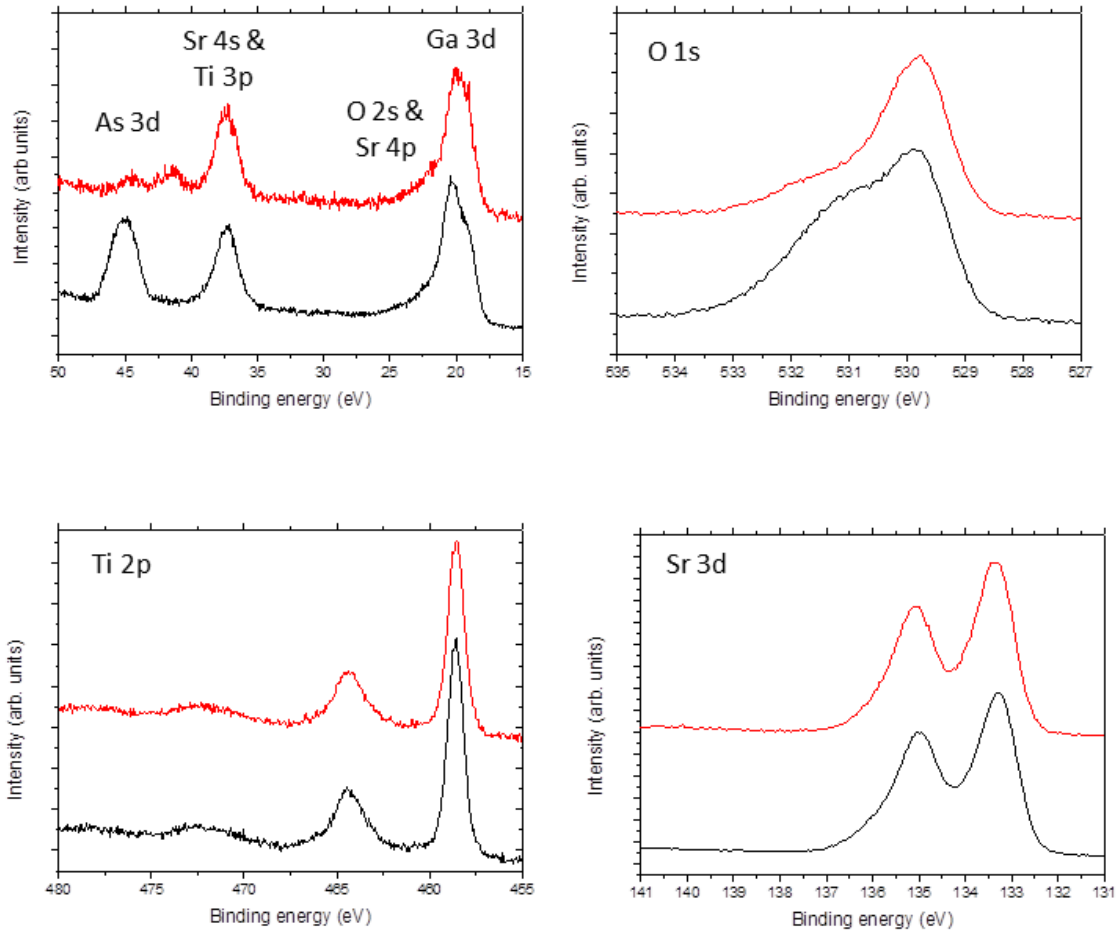

Figure 69. XPS core levels of GaAs / $SrTiO_3$ NWs measured at RT. The black curves correspond to the core levels measured before the annealing, and the red ones are that after the annealing. The photon energy was 750 eV.

2.3. The optical properties of GaAs / $SrTiO_3$ NWs

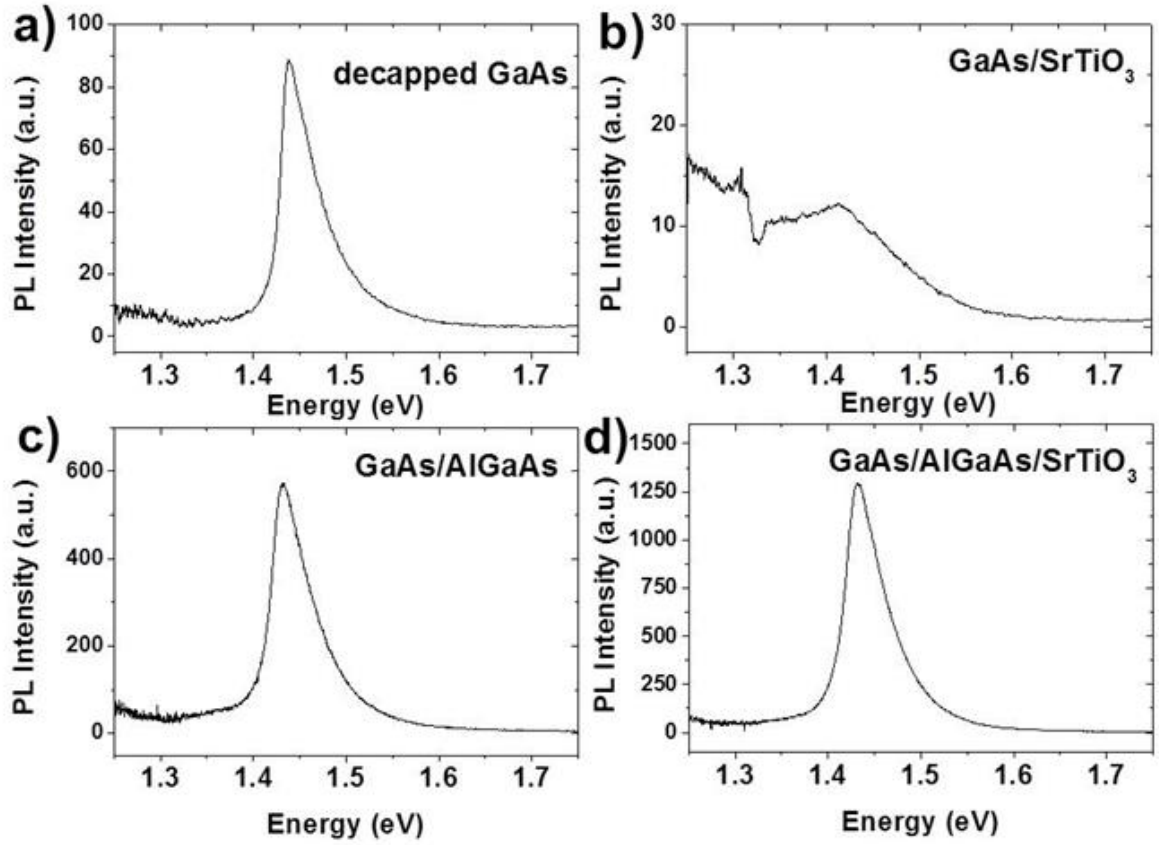

Figure 70. PL spectra of a) decapped GaAs NW array, b) GaAs / $SrTiO_3$ core/shell NW array, c) GaAs / AlGaAs core/shell NW array and d) GaAs / AlGaAs / $SrTiO_3$ core / shell NW array. For sample b) and d) the $SrTiO_3$ was grown using the two-steps method. The measurements were performed at 300 K.

To further probe the properties of this core / shell NW array, PL measurements were implemented (also in collaboration with N. Chauvin INL-INSA). Figure 70 a shows the PL spectrum of GaAs NWs after As cap / decap procedure. The peak located at 1.43 eV is in agreement with the emission energy of the bulk ZB GaAs NWs at RT. Then, the two-steps $SrTiO_3$ growth method was applied to the decapped GaAs NWs under UHV. As shown in Figure 70 b, only a peak of quite low intensity at 1.4 - 1.42 eV might be related to the emission of the GaAs NWs, and a rather low broad band is observed at about 1.25 - 1.3 eV probably originates from defects in the parasitic 3D layer. It should be noted that similar spectra were obtained even though the $SrTiO_3$ shell was grown at lower temperatures. The suppression of PL for this decapped-GaAs (core) / $SrTiO_3$ (shell) NW array could be the consequence of interface defects caused by i) oxidation of GaAs during the $SrTiO_3$ growth (despite the moderate growth temperature and oxygen pressure used during the first growth step) or ii) inter-diffusion of the metallic species (Sr, Ti) into the NWs. To avoid the occurrence of poor light emission properties of the GaAs core, an AlGaAs passivating shell

was grown around the GaAs core. The shape of the PL peak of GaAs / AlGaAs NWs (Figure 70 c) is quite similar to Figure 70 a, but 5 times more intense, showing the efficiency of passivation by this wider band gap material. Finally, GaAs / AlGaAs core / shell NWs were capped with an As layer and then transferred into the MBE chamber dedicated to functional oxides. After the As-decap procedure, the $SrTiO_3$ shell was grown by the two-steps method. An evident strong peak is observed at 1.43 eV (Figure 70 d), in accordance with results obtained before the $SrTiO_3$ growth (Figure 70 c), showing the good optical properties of this GaAs / AlGaAs / $SrTiO_3$ NW array. From time-resolved PL measurements we extracted a lifetime of 300 ps and 209 ps for GaAs / AlGaAs and GaAs / AlGaAs / $SrTiO_3$, respectively (Figure 71). It is well clarified that the AlGaAs passivation can avoid the introduction of non-radiative recombination centers at the GaAs / $SrTiO_3$ interface during the fabrication of the shell.

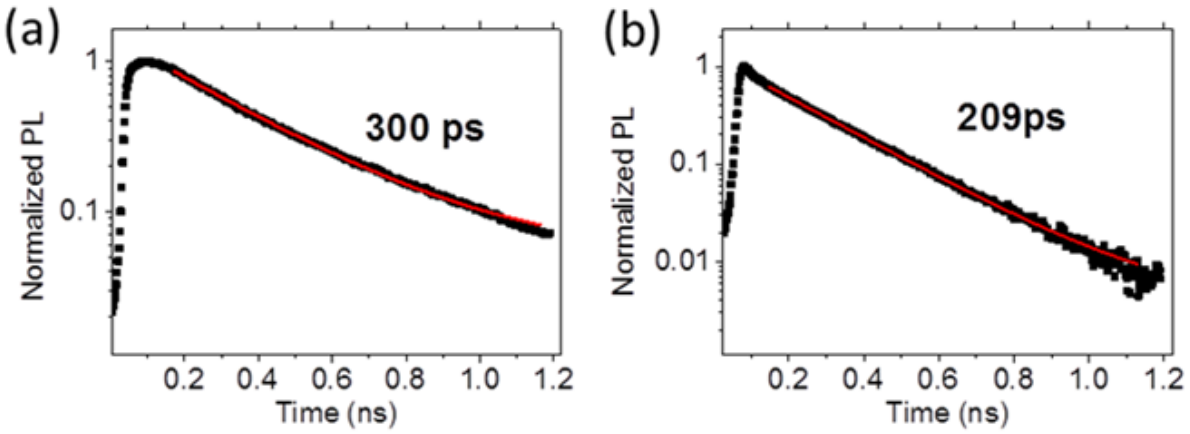

Figure 71. Time-resolved PL measurements for a) GaAs / AlGaAs NWs and b) GaAs / AlGaAs / $SrTiO_3$ NWs. The lifetime was extracted from a mono-exponential decay fitting (red line). Measurements performed at 300 K.

3. Perspective: GaAs / AlGaAs / $SrTiO_3$ / $BaTiO_3$ multishell NWs

In the thin film research field, compared to polycrystalline or amorphous ferroelectric films, epitaxial ones are desirable for their high interface quality and are of major interests for the realization of ferroelectric field effect transistors for non-volatile memories and logic applications.[18] As we discussed in the beginning of this chapter, the epitaxial growth of $SrTiO_3$ on GaAs NWs can open up the route to fabricate functional complex oxides based 1D heterostructures. Hence, the epitaxial growth of core / multishell NWs can be very promising for optimising the crystallography of 1D heterostructures and enhance the physical properties of the practical devices. Chief among them is the prototypical ferroelectric perovskite $BaTiO_3$ that is an attractive candidate for applications such as negative-capacitance field effect devices.[18,56] Thus, we tried to integrate $BaTiO_3$ with GaAs NWs array.

Firstly, 160 ML of $BaTiO_3$ were directly deposited on the surface of the GaAs / AlGaAs NW array at 600 °C. The $BaTiO_3$ growth rate is equal to that of $SrTiO_3$ layer, namely 0.03 ML/s. The as-prepared GaAs / AlGaAs NWs are about 100 nm in diameter with 20 min of GaAs axial growth and 10 min of AlGaAs radial growth. As show in Figure 72 a and b, the diameter of NWs is around 125 nm without any sign of shadowing or tapering for the best ones. The TEM images illustrate the surface morphology of the GaAs / AlGaAs / $BaTiO_3$ NWs (Figure 72 c, d). As expected, the $BaTiO_3$ layer seems to be polycrystalline with a roughened surface. In HRTEM image (Figure 72 e), lattice fringes of different orientations can be clearly seen. Through FFT patterns (Figure 72 f) of the marked zone in Figure 72 e, (100) and (110) plans of $BaTiO_3$ are deduced confirming the existence of $BaTiO_3$. But, as difficult as in the thin film field, the direct growth of $BaTiO_3$ on a GaAs surface was not realized. Consequently, a $SrTiO_3$ buffer shell was used.

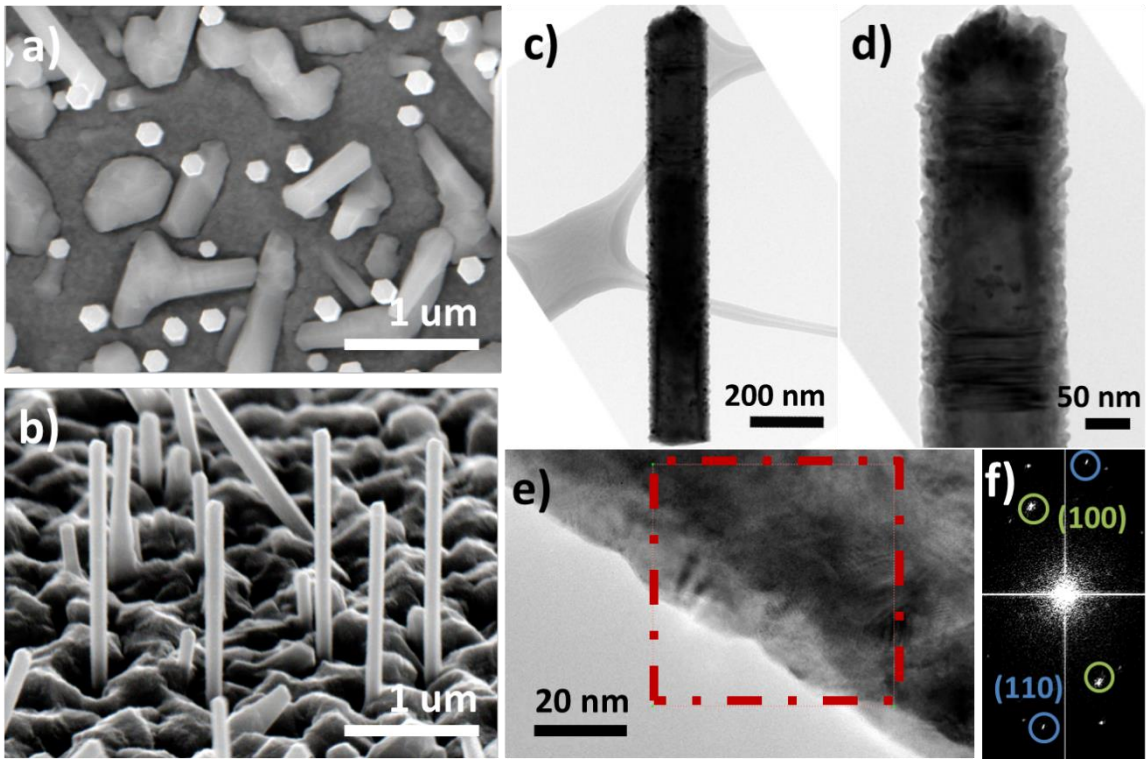

Figure 72. GaAs/AlGaAs/$BaTiO_3$ NWs: a) SEM overview image, b) SEM side view image with 30° tilting, c) and d) typical TEM images, e) HRTEM image and f) its corresponding FFT pattern.

GaAs / AlGaAs / $SrTiO_3$ / $BaTiO_3$ multishell NWs were then grown using the same growth temperature of 600 °C. Their morphology and crystal structure are displayed in Figure 73. The GaAs / AlGaAs NWs were fabricated through the identical procedure as that of GaAs / AlGaAs / $BaTiO_3$ NWs, with 20 min of growth for the GaAs core and 10 min of growth for the AlGaAs shell. The 40ML $SrTiO_3$ layer were grown via the two-steps method. Then 40 ML of $BaTiO_3$ were grown around the GaAs / AlGaAs / $SrTiO_3$ NWs at 600 °C. The final diameter of these multishell NWs is around 115 nm as shown in Figure 73 a and b. From the typical TEM

image in Figure 73 c, we can see that there are nanoparticles attached to the NWs, however, the surface is less rough than that of GaAs / AlGaAs / $BaTiO_3$ NWs shown in Figure 72 d. EDX line scan was implemented along the red dashed line marked in Figure 73 c, confirming that the GaAs / AlGaAs NWs are well packed by oxide shells. It is however not possible to distinguish $BaTiO_3$ and $SrTiO_3$ shells from the EDX scan. It should be noted that the total deposit quantity of $SrTiO_3$ and $BaTiO_3$ is equal, so the $BaTiO_3$ layer should be thinner than the $SrTiO_3$ one due to the increased NW diameter after the growth of $SrTiO_3$.

A higher magnification TEM image reveals the surface morphology of a multishell NW (Figure 73 e). The first observation is that during the growth of $BaTiO_3$, the GaAs NWs keep their identical crystal structure: the ZB and WZ phases as well as the transition section are observed in Figure 73 e. Deduced from the contrast, the thickness of the oxide shell is around 8 nm in total. As we mentioned before, the 40 ML $SrTiO_3$ grown via the two-steps method leads to a $SrTiO_3$ layer thickness around 5 nm. So the thickness of $BaTiO_3$ layer could be about 3 nm. No obvious epitaxial alignment is found based on the results in hand. A more precise HRTEM should be carried on for gathering more information about the oxide crystal orientation.

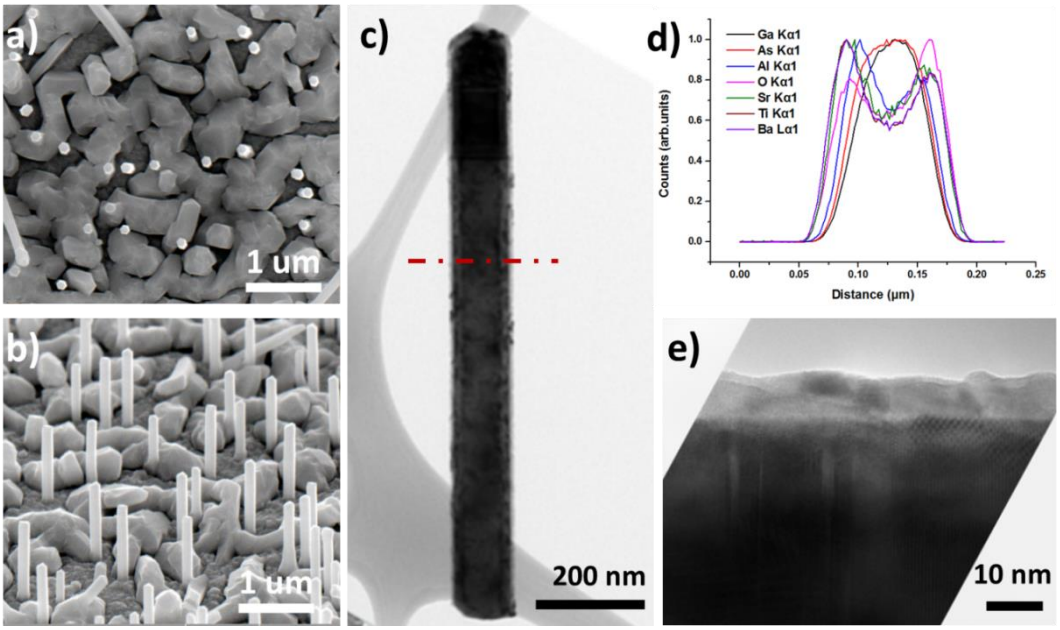

Figure 73. GaAs / AlGaAs / $SrTiO_3$ / $BaTiO_3$ NWs: a) SEM overview image, b) SEM side view image with 45° tilting, c) typical TEM image, d) EDX line scan along the red dashed line marked in c), e) TEM image with a higher magnification.

As aforementioned, the as-grown GaAs / AlGaAs / $SrTiO_3$ NWs have not established fully epitaxial growth. For the extended $BaTiO_3$ layer, epitaxial alignment is expected more difficult to accomplish via a direct growth procedure. So, surface preparation and desorption strategies are indeed needed in order to obtain an abrupt interface free of amorphous interlayer or Ga oxides. The first strategy consists in the preparation of the GaAs NW facets

with Ti, Sr or Zintl-Klemm intermetallic phases.[57] The second strategy consists in growing the functional oxide at temperature high enough for both As oxides and Ga oxides to desorb. Besides, the growth of $BaTiO_3$ is normally applied at high temperature for getting a better crystal structure.[18,58] Concerning the decomposition of GaAs as well as the desorption of Ga and As oxides, a moderate growth procedure of $BaTiO_3$ layer should be used.

It should also be noted that during the radial growth of $BaTiO_3$ on $SrTiO_3$, the strain along the radial direction is different from those in the axial direction as illustrated in Figure 74. Basically, $BaTiO_3$ has a tetragonal structure, and the corresponding lattice parameters are a = 3.994 Å and c = 4.0335 Å (the tetragonal distortion c/a is 1.01; ICDD #83-1880), while the paraelectric cubic phase has a lattice parameter a = 4.006 Å (ICDD #79-2263).[18] Since the lattice parameter a is 3.91 Å for $SrTiO_3$, there is a compressive stress introduced into the $BaTiO_3$ layer. On the contrary, a tensile stress is expected in the $SrTiO_3$ layer. In a NW configuration, the perimeter increases in proportion with the radius. Hence, along the radial direction, the compressive strain coming from the inner $SrTiO_3$ layer may be well released (Figure 74 a). In contrast, along the axial direction, the epitaxial stress is more comparable to that caused by a stacking of two thin layers (Figure 74 b). The compressive strain can't be released easily and could cause further crystallographic defects. So strategies applied in the field of 2D film growth should be borrowed as experiences.

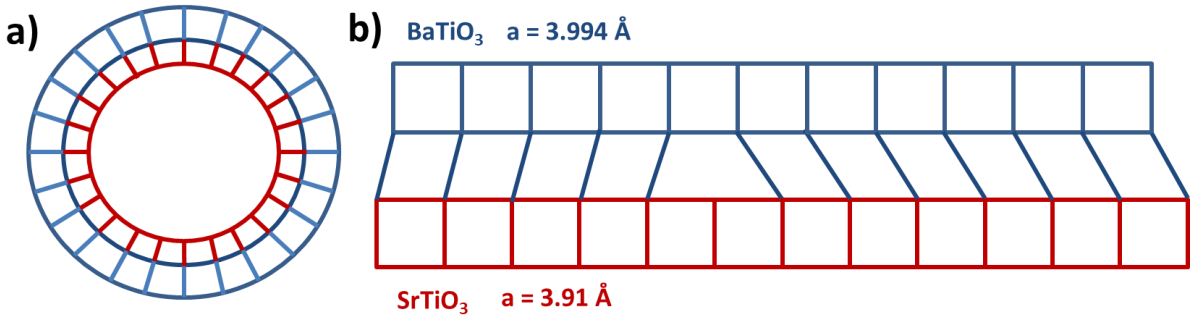

Figure 74. Schematics of lattice matching between $SrTiO_3$ and $BaTiO_3$ along a) the radial direction and b) the axial direction. The lattice of $SrTiO_3$ is labelled in red and blue for $BaTiO_3$.

4. Conclusion

In this chapter, we focus on the growth of GaAs (core) / $SrTiO_3$ (shell) NWs by ss-MBE. Using the As capping / decapping method, the As capped GaAs NWs (or GaAs / AlGaAs NWs) were transferred in air without oxidizing or contaminating of the GaAs (or AlGaAs) facets which is necessary for the further growth of functional oxides. By means of a two-steps method for the $SrTiO_3$ growth, we obtained a partially oriented $SrTiO_3$ shell covering the GaAs NWs. Nevertheless, as revealed by XPS spectra and TEM images, the interface is not abrupt, which probably prevents a perfect epitaxial growth. Through the thermal stability study, it showed that the desorption of the As oxides can be achieved by an annealing under

UHV at around 500 °C. The GaAs / $SrTiO_3$ NWs show a good thermal tolerance, which is positive for the further growth of functional oxides such as the ferroelectric $BaTiO_3$. In summary, our study provides the first evidence that it is possible to obtain monocrystalline epitaxial shell of functional oxides monolithically integrated on semiconducting NWs.

5. References

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Chapter 6. GaAs (core) / oxide (shell) NW array as photoelectrodes for water splitting

1. Introduction

The free energy change (ΔG) for the conversion of one molecule of H_2O to H_2 and 1/2 O_2 under standard conditions is 237.2 kJ/mol, which it corresponds to ΔE° = 1.23 V per electron transferred.[1,2] Using a semiconductor to drive this reaction, the semiconductor must absorb radiant light with photon energies higher than 1.23 eV, *i.e.* light with wavelength equal to or shorter than 1000 nm. The energy will be converted into chemical energy stored in the chemical bonds of H_2 and O_2. This process must generate two electron-hole pairs per molecule of H_2 (2 × 1.23 eV = 2.46 eV) or four electron-hole pairs per molecule of O_2 (4 × 1.23 eV = 4.92 eV). In the ideal case, a single semiconductor material has the E_{CB} and E_{VB} that straddle the electrochemical potentials E° (H^+ / H_2) and E° (O_2 / H_2O), its E_g is large enough to split water. Both HER and OER can be realized, which is also called the over-all water splitting. Semiconductors with wide band gap were hence more studied compared to narrow band gap ones.[3,4] However, the main problem for the wide band gap semiconductor is their low solar light absorption, generally speaking they are more efficient in the UV region than in the other part of the solar spectrum. Semiconductors with narrow band gap can compensate their drawback, and enhance the absorption of the visible and infrared lights. Besides, by sequentially stacking light-absorbing materials with different band gaps, various wavelengths of light in the solar spectrum can be absorbed. It can also provide a sufficient photovoltage as well as high current densities.[5,6]

To carry out the photocatalysis reaction, photoinduced free charge carriers (electrons and holes) in the semiconductor must travel to the semiconductor / liquid junction, and then react with solution species directly at the semiconductor surface. The electron-transfer processes at semiconductor / liquid junctions (SCLJ) produce losses due to the concentration and kinetic overpotentials needed to drive the HER and the OER. Taking the losses into account, the energy required for the water photoelectrolysis at a semiconductor photoelectrode is therefore frequently larger than 1.23 V per photogenerated electron-hole pair.[7] A 1.7 eV / 1.1 eV band gap tandem structure would produce optimal energy-conversion efficiencies that are comparable to those of commercial triple-junction cells obtained with III-V semiconductors.[1]

Several compounds that satisfy the 1.7 eV band gap requirement can be obtained by adjusting the composition of the ternary and quaternary III-V semiconductors.[8] GaAs (E_g = 1.42 eV) herein can serve as a model system to demonstrate the efficiency of III-V NW-array on Si substrate as photoelectrode for water splitting. Subsequently, this NWs-on-Si strategy

could be applied to ternary alloy $GaAs_{0.78}P_{0.22}$ NWs, $Al_{0.20}Ga_{0.80}As$ NWs, or to quaternary alloy NWs that have a 1.7 eV direct band gap.

However, one of the primary problems, which prevents these narrower band gap materials from being utilized as photoelectrodes, is that their surfaces are not photochemically stable.[9] For this type of semiconductors, surface oxidation reaction would compete with the OER, resulting in serious photocorrosion and the formation of insulating surface oxide layers. Even though this issue is less serious for p-type semiconductors under cathodic protection, surface oxidation is still a concern for photocathode under idle conditions or in alkaline electrolytes.[1,10-12] Therefore, passivating their surfaces against photocorrosion without sacrificing their photoconversion efficiency is a promising method to fabricate efficient photoelectrodes.

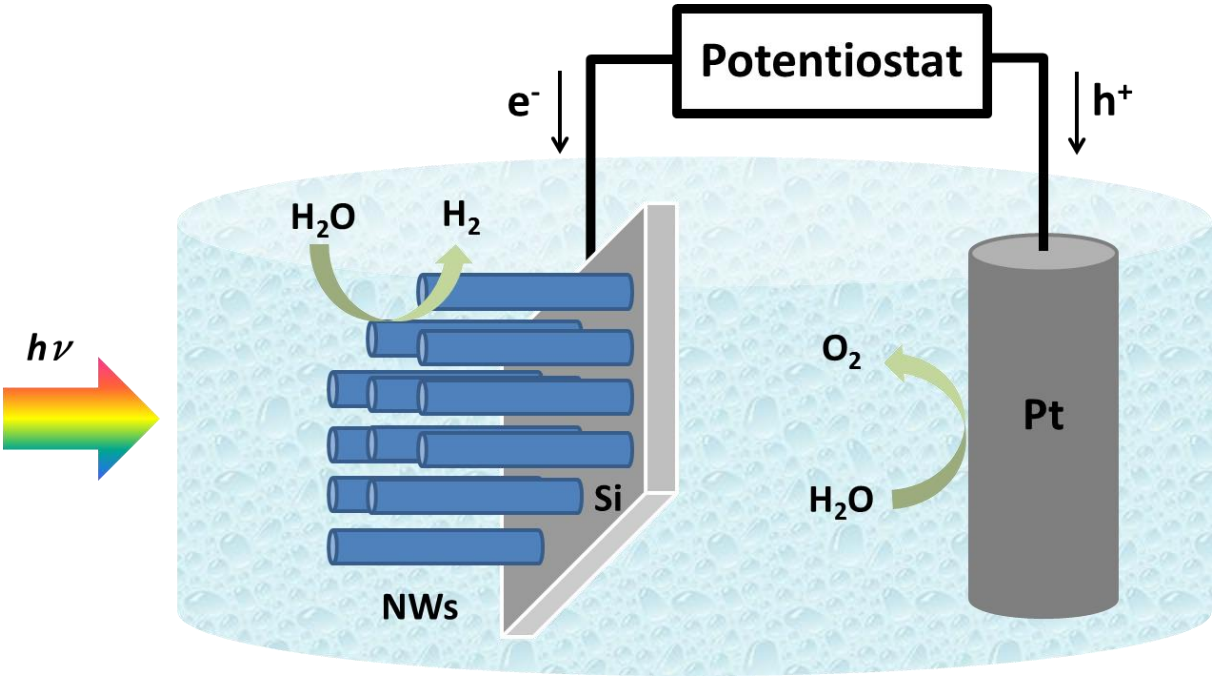

Figure 75. Schematic of a NWs-based PEC cell for water splitting: NWs working as the photocathode, Pt wire serving as the counter electrode and Ag / AgCl electrode as the reference electrode (not shown).

Furthermore, the large surface area of the NWs is expected to increase surface recombinations as more surface states are introduced.[13] Passivation layers have been shown to decrease surface state-mediated charge recombinations.[14,15] Many passivation layers have been studied such as wet chemically deposited sulfide[16] or ligands,[17] III / V shell grown by MOCVD,[17] photoelectrochemically produced oxides,[16,19] and SiN layers produced by CVD.[19] Among all the passivation reported, metal oxides such as TiO_2[21-23] and Al_2O_3[24,25] generally deposited by atomic layer deposition (ALD), are supposed to be the most promising candidates. L. Ji *et al.* reported a Si-based photocathode with a capping epitaxial $SrTiO_3$ layer working as a photocathode for water reduction.[26] The epitaxial $SrTiO_3$ layer

plays the role of passivation layer dramatically improving the stability of the p-Si photoelectrode. Besides the lattice mismatch between Si and $SrTiO_3$ is as small as -1.7%, $SrTiO_3$ is hence one of the few oxides that can epitaxially grow on Si(001) and with minimal interfacial reactions.[27] Hence, crystalline $SrTiO_3$ can be grown on Si with a very low interface state density creating a nearly perfect interface.[28] Photogenerated electrons can be transported easily through $SrTiO_3$ / Si junction because of the perfect lattice matching. Epitaxial $SrTiO_3$ layers are succeded to be grown on the GaAs substrate sharing the structural similarity with Si.[29] Since integreation of monocrystaline $SrTiO_3$ with GaAs in 1D NW is feasible as discussed in Chapter 5, heterogeneous GaAs / $SrTiO_3$ NWs could also be a quite promising photoelectrode.

In this chapter, we present the work on the GaAs NWs-based PEC cell. Figure 75 illustrates the typical PEC cell we used in this work. To enhance the cell performances, the geometry of NWs, especially the length and diameter, was optimized by adjusting the growth parameters by MBE. The effect of the doping concentration was also studied. To avoid the degradation of electrodes caused by the photocorrosion of GaAs NWs, GaAs / $SrTiO_3$ and GaAs / TiO_2 core / shell NW arrays were fabricated. Since a relatively high interface quality is requested, it showed that the structure of GaAs / $SrTiO_3$ NWs needs to be optimized. For the GaAs / TiO_2 NWs, the effect of the thickness as well as the crystallinity of the TiO_2 layer was also investigated. Finally, the effect of Pt nanoparticle co-catalyst was studied.

2. GaAs NWs based photoelectrode

2.1. The influence of the NW diameter

To investigate the effect of NW diameter on the PEC performance of the as-prepared working electrode, three GaAs NW arrays with a different average NW diameter were fabricated by adjusting the radial growth time. The axial VLS growth was set to 40 min for all the three samples. The NW diameter was adjusted by apply different radial growth time, 0, 40 and 60 min, corresponding. The corresponding NW diameter is 50, 130 and 180 nm, respectively (Figure 76 a-c). The average NW length of all three samples is similar, around 2.5 µm.

It is worth noting that the potential presented here is a relative value taking the pH of the electrolyte into consideration, the potential is then converted based on the following equation:

$$V(vs\ RHE) = V(vs\ SHE) + 0.0592 \times pH$$

The solution used for this work is 0.1 M NaOH (pH = 13). The V_{onset} slightly and negatively shifts from 0.52 V to 0.45 V as shown in Figure 76 d. J_{sc}, as defined in Chapter 1, is the current density measured under short-circuit conditions, in our case J_{sc} is obtained at -0.061

V (vs RHE). J_{sc} increases with the enlargement of the NW diameter. This result could be explained by the fact that the surface area progressively increases with the NW diameter.

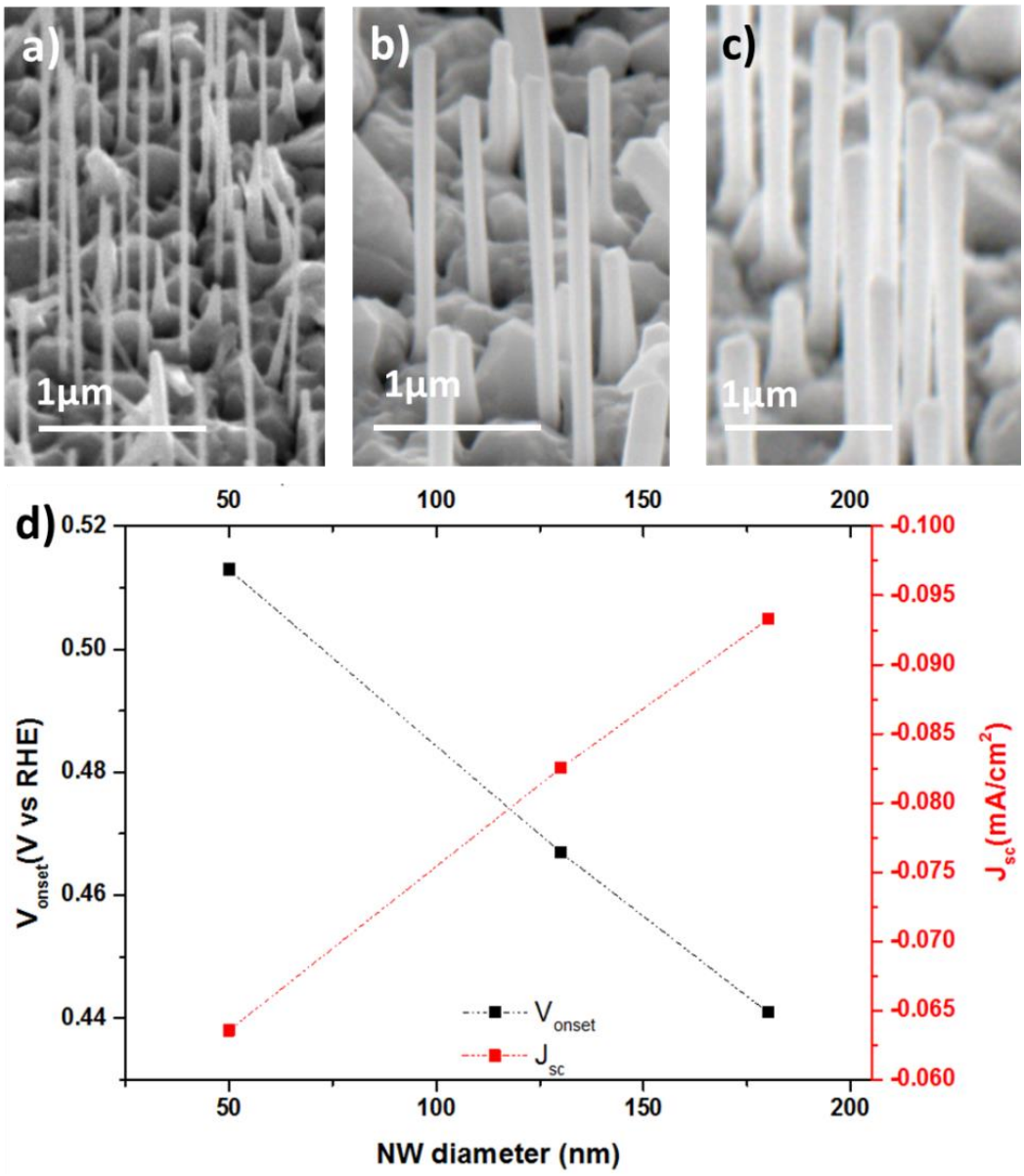

Figure 76. a-c) SEM images of GaAs NW arrays with a different average NW diameter; d) V_{onset} and J_{sc} of NW arrays as a function of the average NW diameter.

2.2. The influence of the NW length

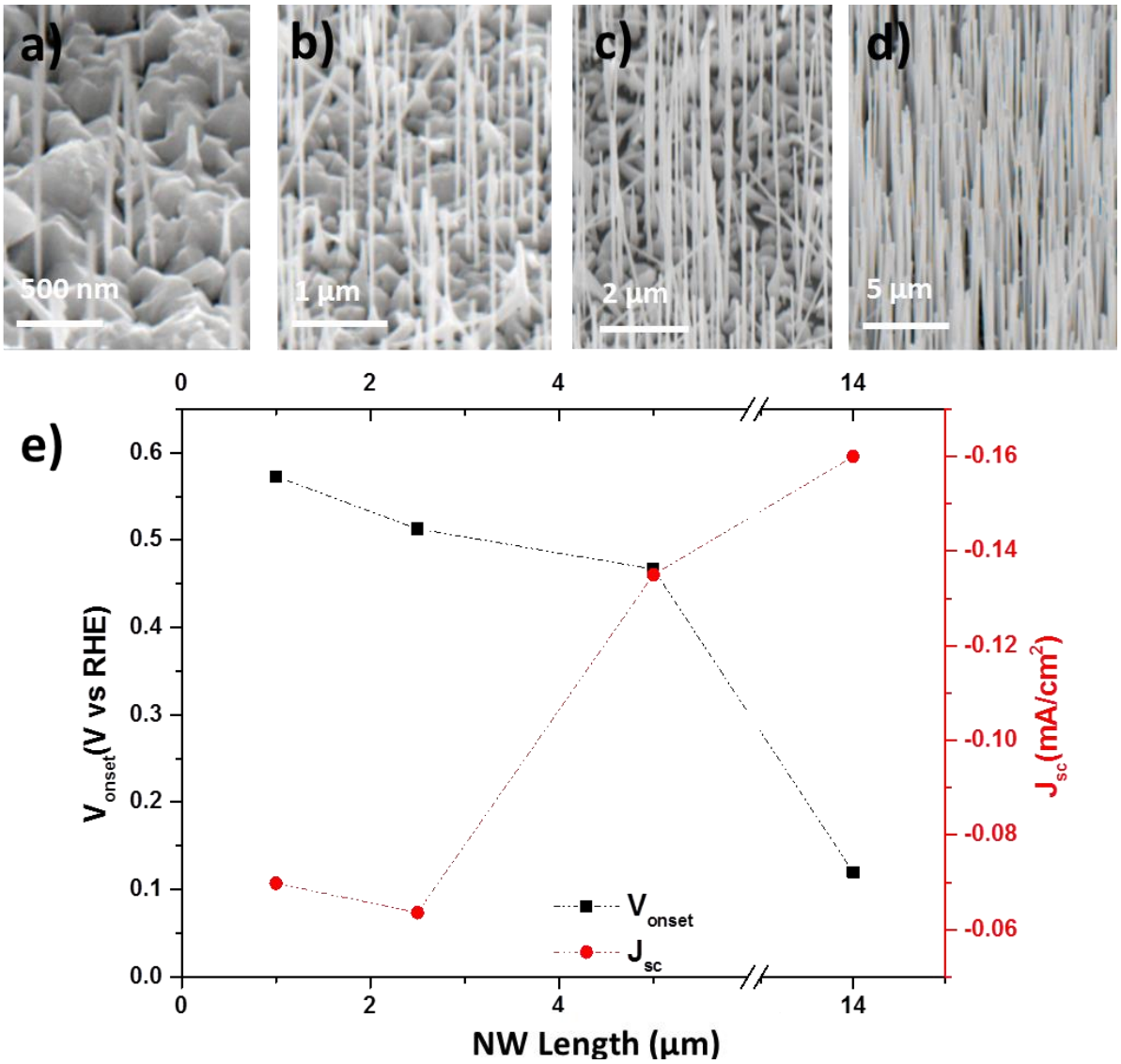

Figure 77. a-d) SEM images of GaAs NW arrays with a different average NW length; e) V_{onset} and J_{sc} of NW arrays as a function of the average NW length.

NWs with different average lengths are studied for investigating the length impact on PEC performances. The average NW length for each sample is 1, 2.5, 5 and 14 µm, respectively, as shown in Figure 77 a-d. The V_{onset} and J_{sc} for these four samples are plotted in Figure 77 e as a function of the NW length. Shorter NWs (1 and 2.5 µm NWs) show lower V_{onset} values but higher J_{sc} on the contrary to the longer ones (5 and 14 µm NWs). The 1 µm-long GaAs NW array shows a low J_{sc} of 0.07 mA/cm^2 and the highest V_{onset} (0.58 V, Figure 77 e). Based on the SEM image, the 1 µm-long GaAs NW array possess the smallest specific surface area of the four samples, hence the least active sites and surface states. However, since the reaction speed is the slowest, the mass transfer in the electrolyte affected the PEC response of 1 µm-long NWs less than that of the other samples with a higher density of active sites.

Hence, the NW array with an average length of 1 µm shows the most positive V_{onset}. In the case of NW array with a length of 2.5 µm, the lowest J_{sc} of 0.065 mA/cm^2 is recorded. The effect caused by the increase of surface states competes with that caused by the increase of active sites, leading a slight decrease of both J_{sc} and V_{onset} (Figure 77 b, e). Concerning the NW array with NWs as long as 5 µm, it shows a notable increase of J_{sc} but a small decrease of V_{onset}. The substrate isn't fully covered, which means less parasitism GaAs crystals, as shown in Figure 77 c. The uncovered position serves as a back reflector, lengthening the path length of photons through the array. So the J_{sc} is enlarged due to the improvement of the incident light absorption as well as the increase of the active sites. The increase of both concentration (reaction related ions can not meet the need because of the slow mass transfer) and kinetic overpotentials (surface states) results into a relatively negative V_{onset} for the 5 µm-long NW array. Prolonging the growth time to 90 min, a NW array with an average NW length of 14 µm was obtained (Figure 77 d). Even if the length of NWs is two times longer than that of the former sample, its J_{sc} merely increases from -0.135 to -0.16 mA/cm^2 while the V_{onset} undergoes a dramatic decrease from 0.48 to 0.11 V (Figure 77 e). Both the overpotential and the surface states are accused for this poor PEC response of the 14 µm-long NW array. In summary, 5 µm seems to be the most favourable length for GaAs NW array.

2.3. The effect of the NW doping

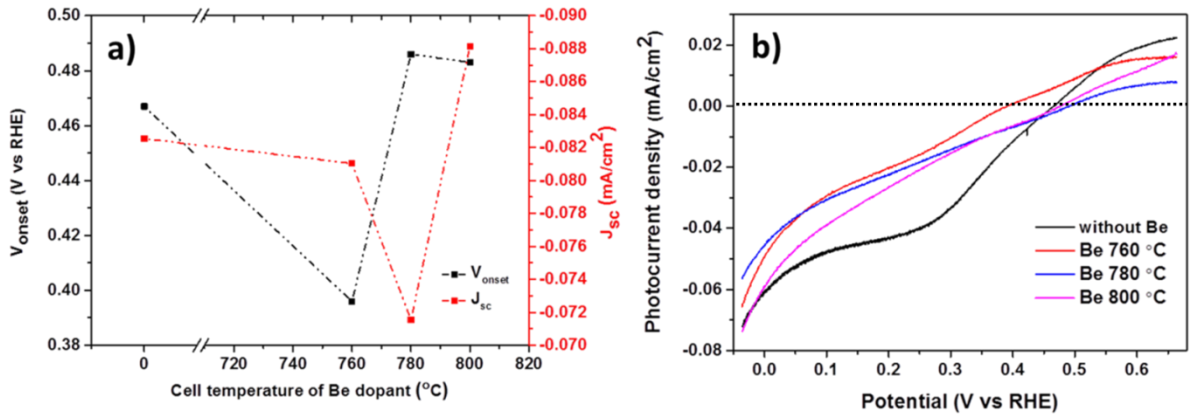

Figure 78. a) The V_{onset} and J_{sc} of NW arrays as a function of the Be dopant cell temperature; b) their corresponding photocurrent density.

To improve the NW conductivity, Be is used as dopant for fabricating p-doped GaAs NW arrays. The quantity of Be dopant is controlled by modifying the temperature of the Be cell in the MBE chamber. The dopant concentration hadn't yet been measured because of the facility limitation. Generally speaking, the higher temperature of the Be cell, the heavier doping is obtained. Four samples were prepared: one intrinsic GaAs NW array, and three others doped with a Be cell temperature (CT) of 760 °C, 780 °C and 800 °C, respectively. The evolution of V_{onset} and J_{sc} with the Be CT is shown in Figure 78 a. There is no clear trend neither for the V_{onset} nor the J_{sc}. The one fabricated with a Be CT of 800 °C presents the

highest J_{sc} (-0.088 mA/cm^2) and a most positive V_{onset} of 0.48 V. The second most efficient one, even though the difference is rather small, is the NW array without Be dopant, presenting a J_{sc} of -0.082 mA/cm^2 and a V_{onset} of 0.47 V. The dark current of all the samples were also recorded. The higher Be CT was set, the larger dark current density is observed. The dark current should be ascribed to the electrode surface oxidation for the more negative VB edge than the O_2 / OH^- redox potential in NaOH solution. Hence, the heavier the Be doping is, the higher possibility for the NW being oxidized. Moreover, the photocurrent density decreases as the doping concentration diminishes as shown in Figure 78 b. It is assumed due to the fact that fewer electrons can be generated within a heavier doped sample even though the conductivity of NW array is enhanced. In Figure 78 b, the intrinsic GaAs NWs show higher photocurrents in the range of 0.01 - 0.45 V. The results are not as expected, more thorough studies need to be done in the future. To simplify the experimental parameters, NWs without dopant are chosen in the following studies.

2.4. The typical GaAs NW array for PEC cells

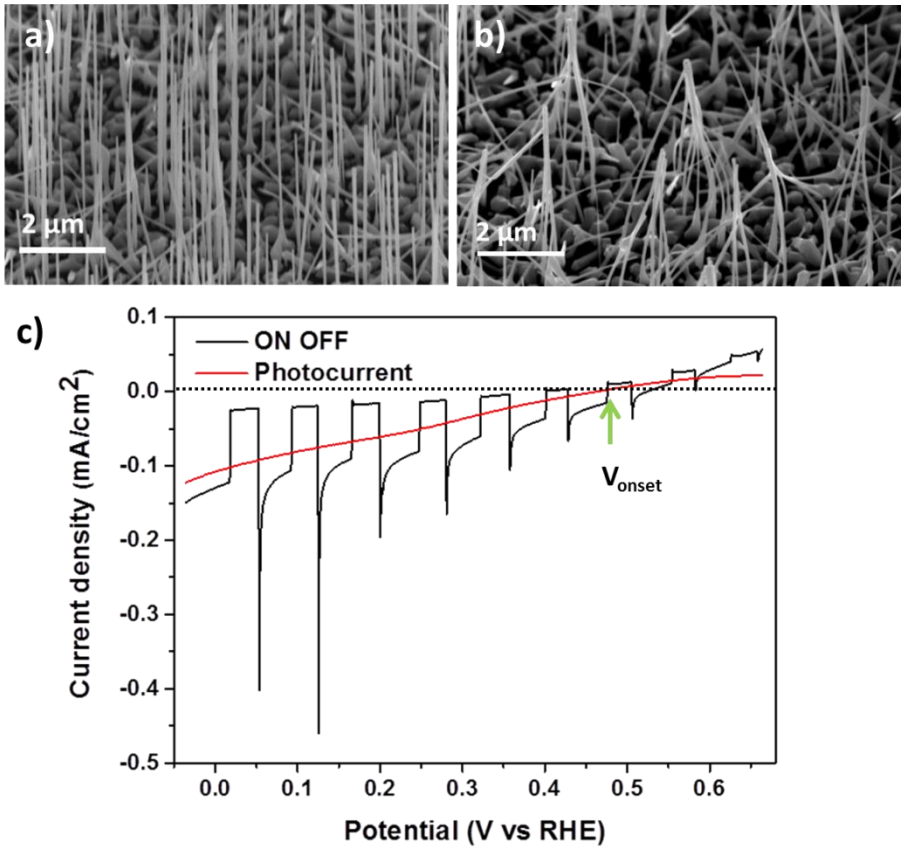

Figure 79. SEM images of the GaAs NW array before a) and after b) PEC measurements; c) ON-OFF curve and photocurrent density curve. V_{onset} is indicated by the green arrow in c).

Considering the results obtained (sections 2.1-2.4), we optimized the NW array configuration: 75 nm in diameter, 5 µm in length, without dopant. p-Si (111) wafers were

used as substrates for the NW array growth (Appendix 3). The protocol of sample preparation is described as follow.

The substrate was firstly ultrasonically cleaned in ethanol and acetone before introduced into the UHV system, each for 5 min, to remove surface contaminations. The pre-deposition temperature and growth temperature (read from the pyrometer) for the p-type Si substrate were higher than that of the n^+ Si(111). 1 nominal ML of Ga was deposited on the substrate at 530 °C (T_{py}) with a Ga flux of 0.50 ML/s. The substrate temperature was then increased to 610 °C (T_{py}) for the growth of GaAs NWs. The Ga flux was set to 0.75 ML/s. The $R_{V/III}$ was equal to 10. After 20 min, the Ga flux was shuttered and the sample was cooled down to RT under an As_4 flux to avoid the GaAs decomposition. In order to grow NWs with larger diameter, after the 20 min axial growth, the temperature of the sample was decreased to 490 °C (T_{py}) under an As_4 atmosphere to switch to the radial growth mode.

A typical NW is 75 nm in diameter and 5 µm in length in average (Figure 79 a). The NW array possesses a relatively low NW density, around 1.8 NW/µm^2. Parasitic GaAs crystals are also observed on the surface of the Si substrate, while some parts of the Si substrate surface are stilled uncovered. For one representitive NW array, merely 0.7% of the surface area of the Si substrated is covered by GaAs NWs, equal to the material mass of one 40 nm-thick GaAs film growing on the same substrate. Most of the NWs are vertical to the surface of the substrate, showing good epitaxial relationship with the p-type Si(111) substrate. After the PEC measurements, NWs are obviously bended and bunch together, especially the longer ones. Each cluster contains 5-10 NWs. Besides, more Si surface is exposed after the PEC test, revealling the degradation of bare NW array.

Since the p-type Si(111) substrate scarcely responds to the illumination (Appendix 3) within the potential window from -0.033 to 0.67 V (vs RHE), the notable response to light detected in Figure 79 c is attributed to the GaAs NW array. The J_{sc} is about -0.135 mA/cm^2, and the V_{onset} is -0.47 V vs RHE. The transient current is observed again due to the slow kinetic of the reaction. A sharp cathodic current spike appears because the light was turned on, and then the current density decays as the accumulation process perturbs the charge distribution of the space charge region until equilibrium is eventually reached between water reduction and charge recombinations. No anodic transient peak is observed when the light was turned off, which means that photogenerated electrons barely accumulated at the SCLJ. Because of the large surface-to-volume ratio of NWs, surface states are considered as the primary trapping centers for photoexcited carriers.[30] H. Joyce *et al.* reported that GaAs NWs has higher surface recombination velocities as 10^5 cm/s and lower electron mobilities as 10^3 cm^2/Vs, and the carrier life time shows serious dependence on the diameter of NWs.[31] Hence, the existence of a cathodic transient current in the case of GaAs NW array should be attributed to the high density of surface trap states. The relatively low photocurrent density is due to the low surface coverage and the impeded carrier transport at the GaAs / Si interface.[30]

IPCE measurements are carried out under a monochromatic light, at a bias of 0.033 V vs RHE. For these measurements, we used a Cornerstone 130 model 74004 monochromator (Newport). The wavelength was varied between 300 and 1000 nm, with a step interval of 10 nm. From the spectrum of IPCE, it can be seen that light is absorbed when the wavelength is less than 900 nm, equivalent to a band gap larger than 1.38 eV (Figure 80). It is also proved that the absorption is ascribed to the GaAs NWs (E_g=1.42 eV) rather than the Si substrate (E_g=1.1 eV).

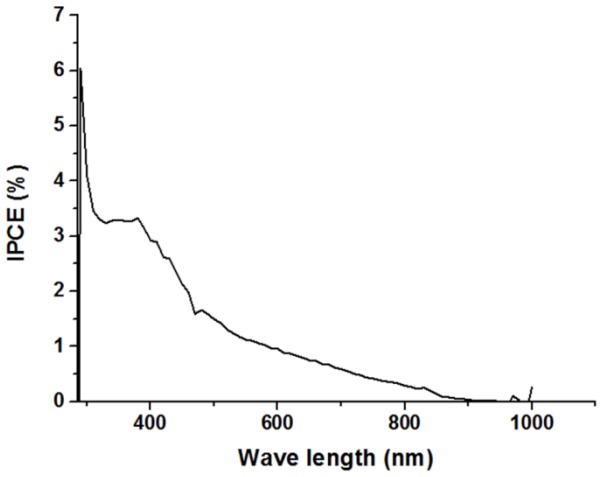

Figure 80. IPCE spectrum measured at 0.033 V vs RHE.

3. GaAs core / oxide shell NWs based photoelectrodes

Because of the poor stability of narrow band gap semiconductors in aqueous electrolytes, especially under basic conditions, the study on narrow band gap semiconductor based photo-electrodes is focused on the photocathode working in acid solutions.[32-34] It was found that the dissolved O_2 concentration must be less than 15 ppb to prevent p-type Si from oxidation, which is unfeasible for practical applications.[1] Hence, a surface protection layer is needed to passivate the electrode. Even though the GaAs electrode is quite intriguing as a model system, so far, only S. Hu *et al.* reported the solar energy conversion properties of a GaAs NW array as a photoanode in non-aqueous solvents to simplify the analysis of the kinetic process (one-electron and reversible reaction).[8] As we discussed before, metal oxides are one of the most promising passivation layer materials. In this section, we present the preliminary results on the fabrication and characterization of GaAs / oxides NWs, as well as their PEC performances.

3.1. GaAs / $SrTiO_3$ NWs

L. Ji *et al.* has reported the study on the p-type Si(001) substrate protected by a four-unit-cell (ca. 1.6 nm) MBE-grown $SrTiO_3$ layer as for H_2 production than for the PEC photocathode.[26] The alignment between the CB of $SrTiO_3$ and that of Si could facilitate the

electron conduction. Besides, other features also improve the PEC performances of this hybrid system, such as the single crystalline nature of this $SrTiO_3$ layer, a lattice mismatch as small as -1.7% with Si(001), as well as a high-quality $SrTiO_3$-Si epitaxial interface with reduced recombination centers.

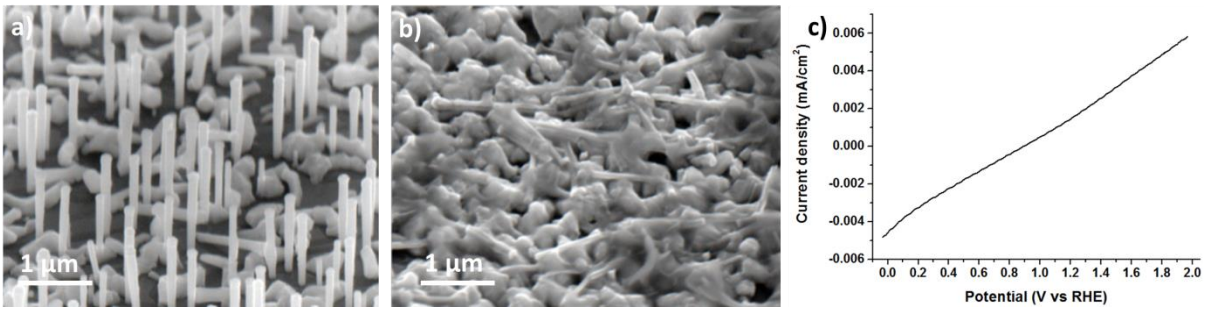

Figure 81. SEM images of GaAs / $SrTiO_3$ NW array a) before and b) after the PEC measurements; c) ON-OFF chopped illumination curve obtained for GaAs / $SrTiO_3$ NWs.

Since it is possible to fabricate an epitaxially grown GaAs / $SrTiO_3$ core / shell NW array as we presented in Chapter 5, GaAs / $SrTiO_3$ core / shell NW array could be quite promising when applied into PEC devices. Hence one GaAs / $SrTiO_3$ NW array was prepared through the procedure mentioned in Chapter 5, with a NW average diameter of 100 nm and NW average length of 1 µm, as shown in Figure 81 a. Its ON-OFF curve is illustrated in Figure 81 c, which shows no PEC response. The NWs were destroyed after the PEC test as presented in Figure 81 b. We assumed that partially epitaxial grown $SrTiO_3$ could not offer stubborn enough protection for the GaAs core, and a more reasonable applied potential window and a more appropriate electrolyte could improve the PEC response. The integration of GaAs / $SrTiO_3$ is still under optimizing in order to obtain a high quality heterostructured NW array. Even though the first trial is unexpectedly failed, the perspective is believed rather bright.

3.2. GaAs / TiO_2 NWs

3.2.1. TiO_2 shell grown by MBE

Taking advantage of the former studies on functional oxides constructed by MBE in our lab, TiO_2 was deposited by MBE in order to get a conformal shell (Figure 82 a) protecting the GaAs NW array from corrosion and passivating the surface states during the PEC measurements. The GaAs NW array was transferred under UHV to another MBE reactor dedicated to oxides for the TiO_2 deposition. The TiO_2 deposition rate was about 1.84 ML/min, and the O_2 partial pressure was set as 5×10^{-8} Torr. During the deposition, the sample was maintained at a temperature of 150 °C to obtain an amorphous TiO_2 shell. The expected thickness of the TiO_2 layer is about 5 nm for a 20 min deposition. The diameter change of NWs before and after the deposition of TiO_2 is not detectable from the SEM images. Further HRTEM measurements are needed to obtain the precise value of the TiO_2 layer thickness. No

NW cluster is detected after the PEC measurements as shown in Figure 82 b, which means that the GaAs / TiO_2 NWs show higher tolerance to the electrolyte than the bare one.

For a GaAs / TiO_2 NW array, only a small transient current was detected when the light was turned on (Figure 82 c, marked with blue dashed circle). Moreover, in the case of GaAs / TiO_2 NW the dark current is closer to 0 than that of the bared one (Figure 82 d), which might be attributed to the better resistance. However, the current density decreases almost 40% after the passivation (Figure 82 c), probably due to the insulating behaviour of the TiO_2 layer. Thinner TiO_2 layer deposited by ALD might improve the performance of the electrode. The V_{onset} of GaAs / TiO_2 NW arrays is more positive than their bare NW arrays counterparts, which could benefit the efficiency of the practical cell in the future.[2] As TiO_2 is intrinsically an n-type semiconductor, its Fermi level stays close to the CB edge, therefore the $E_{qF,e}$ of the GaAs should align approximately with the conduction band of TiO_2, causing the increase of V_{ph}.[13] Since the adding of the TiO_2 layer also caused the change of overpotential. Further study is needed to understand if the V_{ph} is improved.

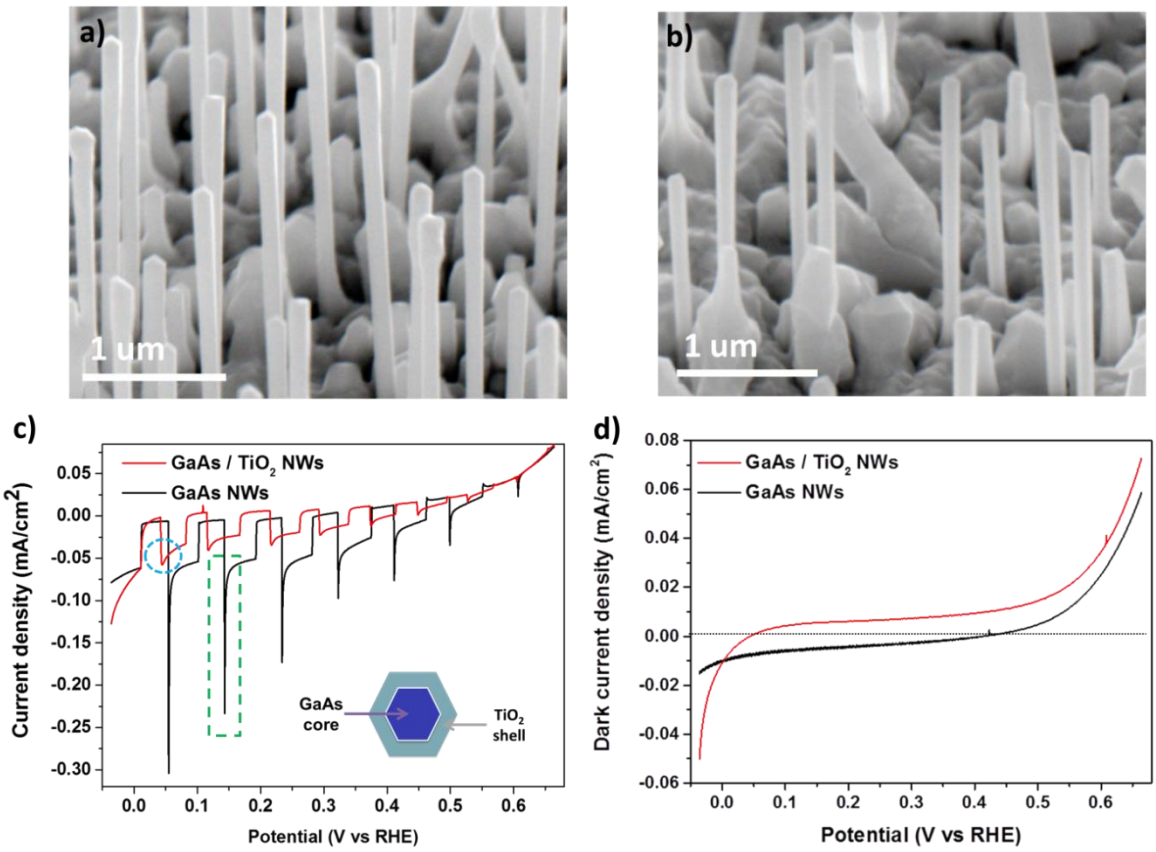

Figure 82. SEM images of the GaAs / TiO_2 NW array a) before and b) after the PEC measurements; c) the ON-OFF chopped illumination curves obtained for GaAs / TiO_2 NWs and bare GaAs NWs; d) the dark current density of GaAs / TiO_2 NWs and bare GaAs NWs. The insert in c) is the cross section schematic of the GaAs / TiO_2 NWs.

3.2.2. The thickness of TiO_2 (deposition time)

Since TiO_2 is a semiconductor, whether the TiO_2 deposition will affect the charge transfer of the system even though it is rather effective against the photocorrosion? Generally speaking, there are three mechanisms to interpret the conductivity of a TiO_2 photoelectrode: the hole conduction mechanism of thick TiO_2 (*i.e.*, defect state-based),[35] the electron transport by CB alignment for thick TiO_2 as well,[36] and the tunnelling effect for thin TiO_2 layer.[37] Hence there are different carrier paths for TiO_2 layers of different thickness. In this section, we focused on the thickness effect of the MBE grown TiO_2 layer on the PEC performances.

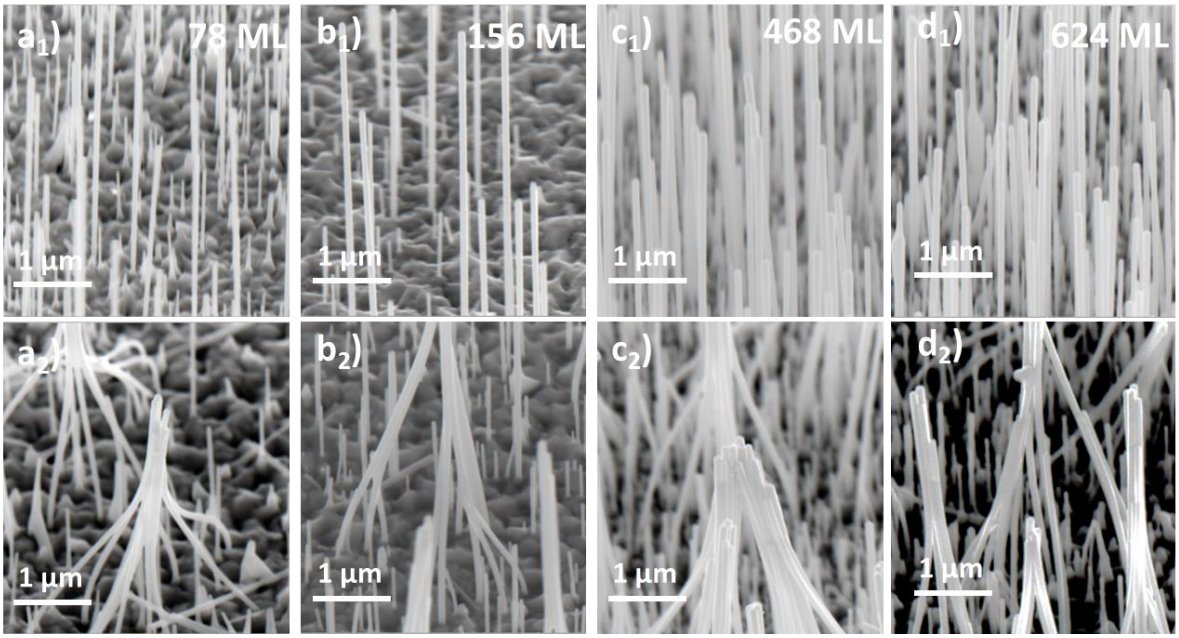

Figure 83. SEM images of GaAs / TiO_2 NW arrays with different TiO_2 thickness: a) 78 ML, b) 156 ML, c) 468 ML and d) 624 ML; a_1-d_1) before PEC measurements, a_2-d_2) after PEC measurements.

GaAs / TiO_2 core shell NW arrays were prepared for different TiO_2 deposition times, in order to tune its thickness. The sample temperature was fixed at 150 °C during the deposition and the sample was cooled down to RT after the growth. Since TEM measurements hadn't been performed due to facility limitations, the exact thickness of TiO_2 for each sample is unknown. Instead of the thickness, the corresponding nominal ML value of the TiO_2 deposition is used. Four samples were prepared: same GaAs core and TiO_2 shells with different thickness, 78, 156, 468 and 624 ML of TiO_2, respectively. Figure 83 shows the SEM images of GaAs / TiO_2 NW arrays with different TiO_2 thickness. The difference in NW density is because of the irreproducibility of the NW MBE growth. From Figure 83 a_1 to d_1, the average diameters of NWs are 50, 55, 80 and 78 nm, the deviation is also ascribed to the irreproducibility of the NW MBE growth. Figure 83 a_2 to d_2 are the corresponding SEM images after the PEC measurements. Bunched NWs are observed for all of the four samples

after the PEC tests. The bunching phenomenon is assumed as the consequence of the contact with the electrolyte and thus to the degradation of the NWs. Long NWs are inclined to bunch together as expected. Further morphology and elemental analyses should be performed to understand the electrode degradation.

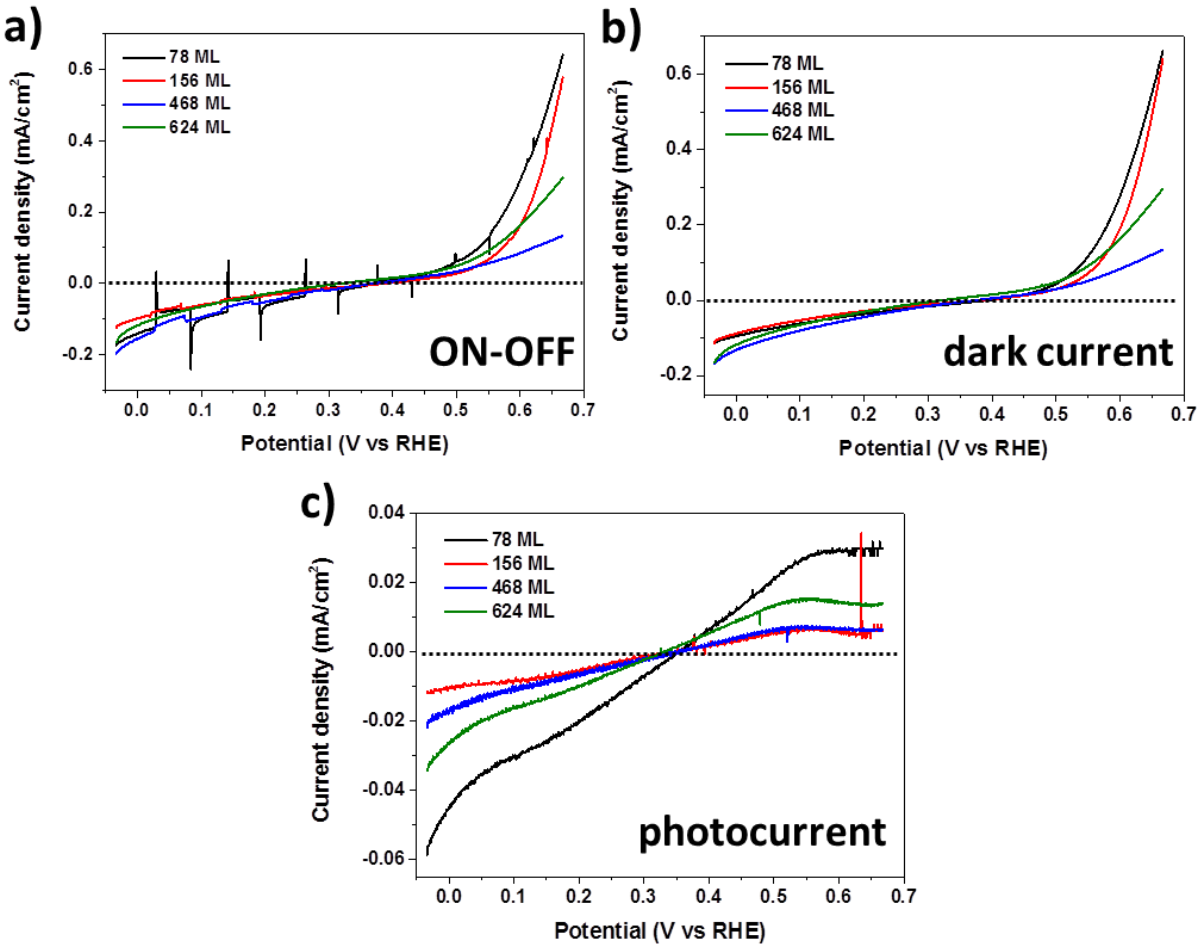

Figure 84. a) ON-OFF chopped illumination curves obtained for GaAs / TiO_2 NW arrays with different TiO_2 thickness; their corresponding b) dark current density and c) photocurrent density.

The corresponding PEC performances are presented in Figure 84. The linear sweep voltammetry (LSV) was conducted at an applied potential window from 0.033 V to 0.670 V. The NW array with a 78 ML of TiO_2 layer shows the most obvious stair case shaped curve when a chopped illumination is applied, even though the transient current is much more serious than all the other three samples (Figure 84 a). It is hence the one with 78 ML that yields the highest photocurrent among the four samples (Figure 84 c). Concerning the dark current, the value is similar for all of the four samples (Figure 84 b). So, for a TiO_2 layer deposited by MBE, a thin layer is preferred. Further explanations to understand the conduction mechanism are however needed.

3.2.3. The crystallinity of TiO_2 (annealing temperature)

The defects within the TiO_2 layer and the interface between TiO_2 and GaAs can either serve as recombination centers for the charge carriers or improve the conductivity of the TiO_2 layer. The O vacancies within the TiO_2 layer can further provide catalytically active sites for the absorption of PEC related ions.[35] A balance among all the effects mentioned should be found to optimize the PEC performance of GaAs / TiO_2 NW arrays. Hence, apart from the thickness, the crystallinity of TiO_2 was also studied.

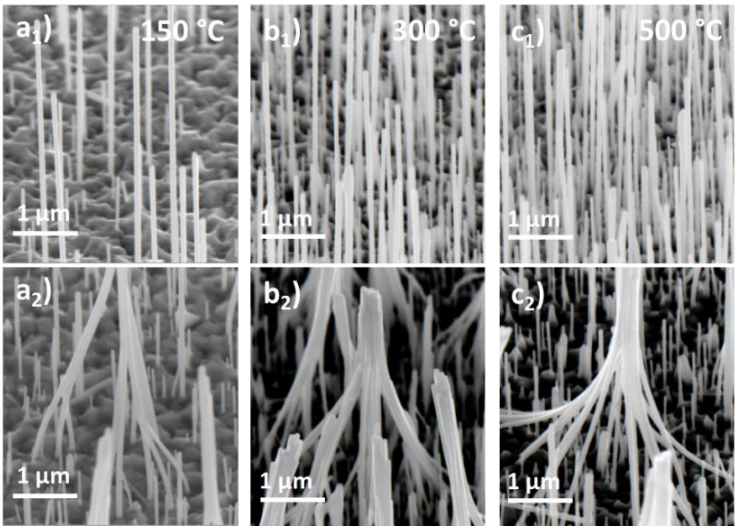

Figure 85. SEM images of GaAs / TiO_2 NW arrays with different TiO_2 deposition temperatures: a) 150 °C, b) 300 °C and c) 500 °C; a_1-c_1) before PEC measurements, a_2-c_2) after PEC measurements.

The rate and quantity (78 ML) of TiO_2 deposition was identical for all the three samples, only the annealing temperature was changed, 150, 300 and 500 °C, respectively. Figure 85 a_1-c_1 show SEM images of GaAs / TiO_2 NW arrays with different TiO_2 deposition temperatures. The NW diameter is around 55 nm for all the 3 samples and the annealing didn't change the NW diameter. The NW morphology after the PEC tests is shown in Figure 85 a_2-c_2. The similar bunching phenomenon is observed. Their corresponding PEC performances are presented in Figure 86. The annealing increases the transient current due to the slow reaction kinetic (Figure 86 a). The difference of dark current is negligible as shown in Figure 86 b. The NW array with TiO_2 deposited at 300 °C possesses the highest photocurrent. However, more studies should be done to investigate the effect of TiO_2 crystallinity.

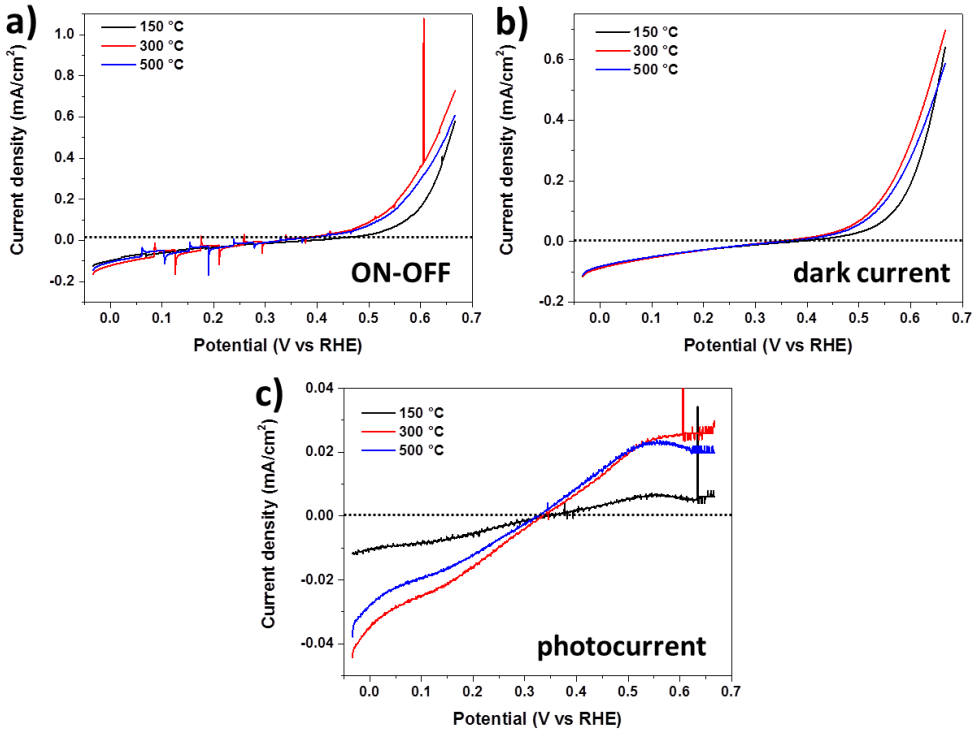

Figure 86. a) The ON-OFF chopped illumination curves of GaAs / TiO_2 NWs obtained with different TiO_2 deposition temperatures; b) their corresponding dark current density and c) photocurrent density.

3.2.4. Pt nanoparticles serving as co-catalyst for water splitting

To improve the PEC performances, platinum (Pt) particles were deposited as co-catalyst. Pt particles were grown by Plasma Enhanced ALD from the (methylcyclopentadienyl)-trimethyl platinum (MeCpPtMe3) precursor (pulse and purge durations of 1 s and 10 s, respectively). Four different samples were prepared, one bare GaAs NW array, one GaAs / Pt NW array, one GaAs / TiO_2 NW array and one GaAs / TiO_2 / Pt NW array. It should be noted that the both Pt and TiO_2 layers mentioned in this section were as thick as 30 ML deposited by ALD while the sample temperature was set at RT. The STEM image of one typical GaAs / TiO_2 NW is shown in Figure 87 a. The thickness of the amorphous TiO_2 layer is around 20 nm. The high angle annular dark field (HAADF) image shown in Figure 87 b is corresponding to the marked area in Figure 87 a. The electron energy loss spectroscopy (EELS) elemental mapping under STEM mode (Figure 87 c-g) revealed the spatial element distributions of Ti, O, Ga and As. Ti and O were concentrated at the NW edge while Ga and As were in the inner part of the NW. The element distribution is in good agreement with the GaAs / TiO_2 configuration. The presence of Pt is proved by XPS spectra measured for the GaAs / Pt NW array and the GaAs / TiO_2 / Pt NW array (not shown here).

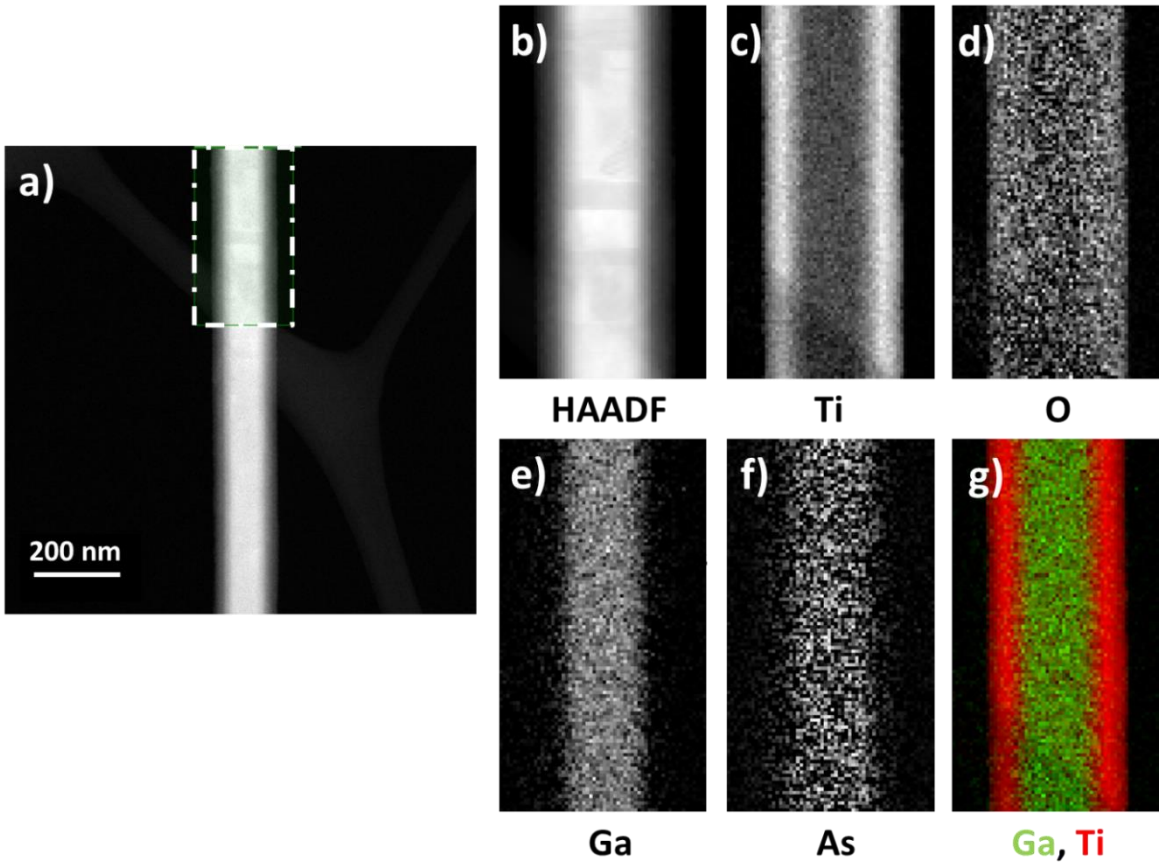

Figure 87 a) STEM image of one typical GaAs / TiO_2 NW; b) HAADF image of the selected area of the NW in a); c-g) EELS mapping for the different elements.

Their corresponding PEC performances are presented in Figure 88. From the LSV curves, the bare GaAs NW array and the GaAs / Pt NW array can work as photocathode, while the GaAs / TiO_2 NW array and the GaAs / TiO_2 / Pt NW array could serve as photoanode (Figure 88 a). The dark current is similar for the different samples, only the one of the GaAs / Pt NW array is slightly larger than the others (Figure 88 b). The V_{onset} is around 0.24 V vs RHE for the bare GaAs NW array and the GaAs / Pt NW array, 0.12 V for the GaAs / TiO_2 NW array and 0.18 V for the GaAs / TiO_2 / Pt NW array (Figure 88 c).

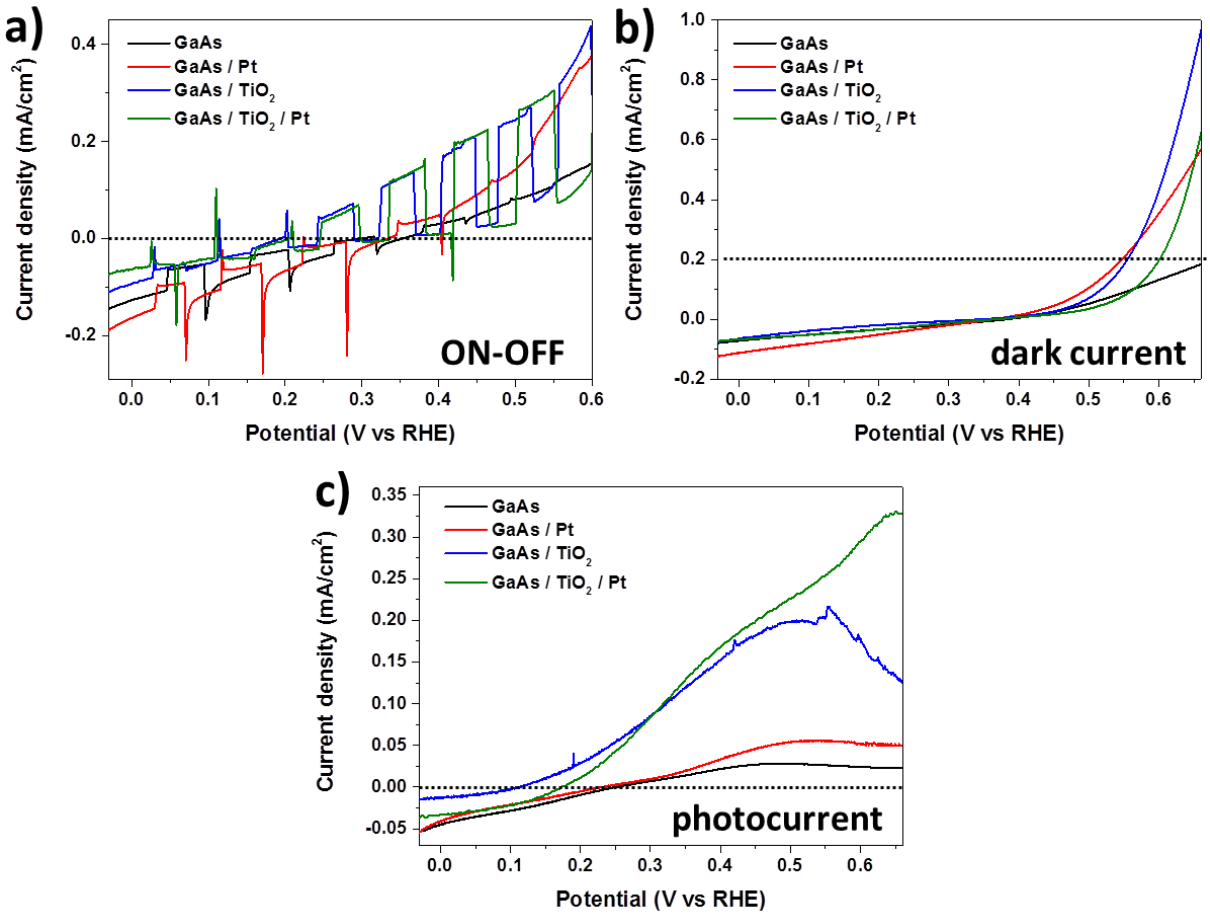

Figure 88. a) ON-OFF chopped illumination curves obtained for the bare GaAs NW array (black), the GaAs / Pt NW array (red), the GaAs / TiO_2 NW array (blue) and the GaAs / TiO_2 / Pt NW array (green); their corresponding b) dark current density and c) photocurrent density.

To check the stability of the electrode, a 1 h LSV test has been performed to the bare GaAs NW array and the GaAs / TiO_2 / Pt NW array at a given V_{ab}, -0.03 and 0.52 V vs RHE, respectively. Before the PEC test, their morphology was observed by SEM as shown in Figure 89 a_1 and b_1. At -0.03 V, GaAs NWs working as the photocathode, a negative current density should be obtained. The absolute value is given here for comparison. Its current density drops dramatically in the first 250 s from 0.12 to 0.065 mA/cm^2 (Figure 90). Then it recovers gradually. At the end of test (1h), the current density is back to 0.115 mA/cm^2 even though the majority of NWs are destroyed (Figure 89 a_2). For GaAs / TiO_2 / Pt NW array, a positive current was measured and attributed to the OER at 0.52 V. The evolution of the current density was recorded as a function of time (black curve in Figure 90). It decreases steadily during the stability test from 0.22 to 0.17 mA/cm^2, which is equal to a 20.4 % shrink of the current density in one hour. Moreover, it is worth noting that, based on the SEM image, the NW are well preserved after the stability test (Figure 89 b_2).

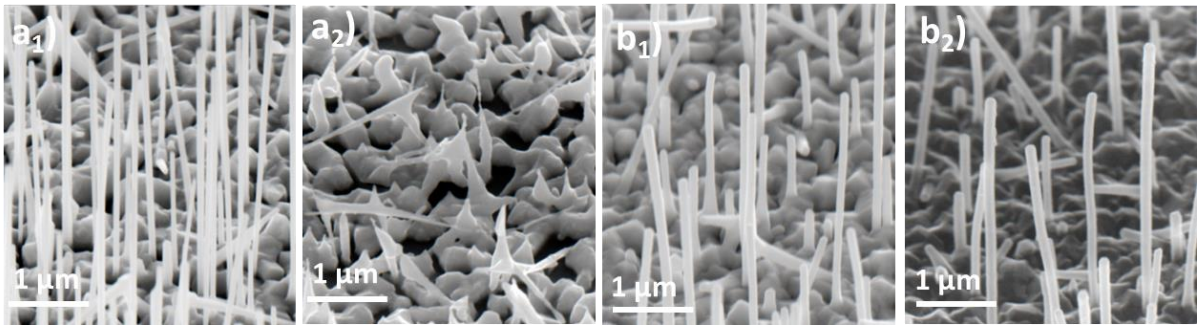

Figure 89. SEM images of GaAs NWs a) without and b) with a TiO_2 layer, a_1-b_1) before the stability test, a_2-b_2) after the stability test.

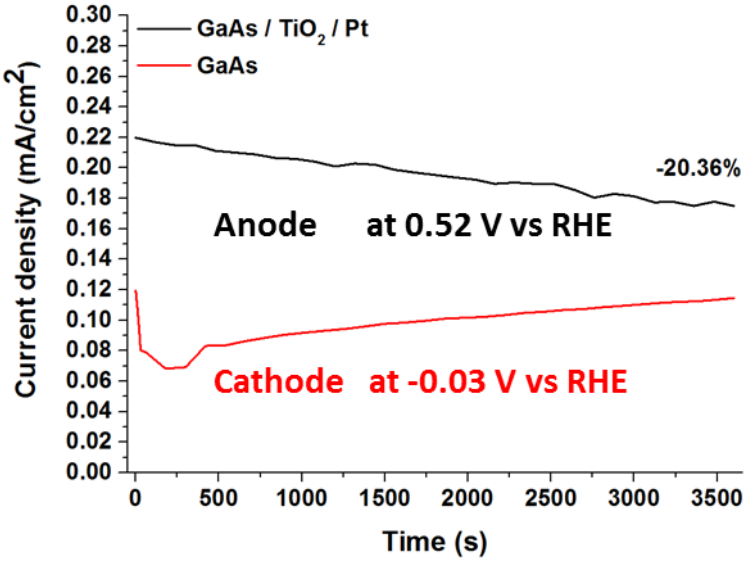

Figure 90. Stability tests for the bare GaAs NW array and the GaAs / TiO_2 / Pt NW array.

The performances before and after the PEC test are measured for both samples in Figure 91. After the aging test, the bare GaAs NW array shows better performances than before in the applied potential window of -0.08 - 0.67 V, presenting a lower dark current density (Figure 91 a, c), a more positive V_{onset} and a bigger photocurrent density value (Figure 91 e). In the case of the GaAs / TiO_2 / Pt NW array, it could work as both photocathode and photoanode after the aging test, while its attribution to HER was negligible before (Figure 91 b, f). The dark current density of an aged sample is always higher than the unaged one (Figure 91 d). The photocurrent density of the aged sample is higher if the V_{ab} is less than 0.09 V or larger than 0.31 V, and lower than the unaged one if 0.09 V < V_{ab} < 0.31 V (Figure 91 f).

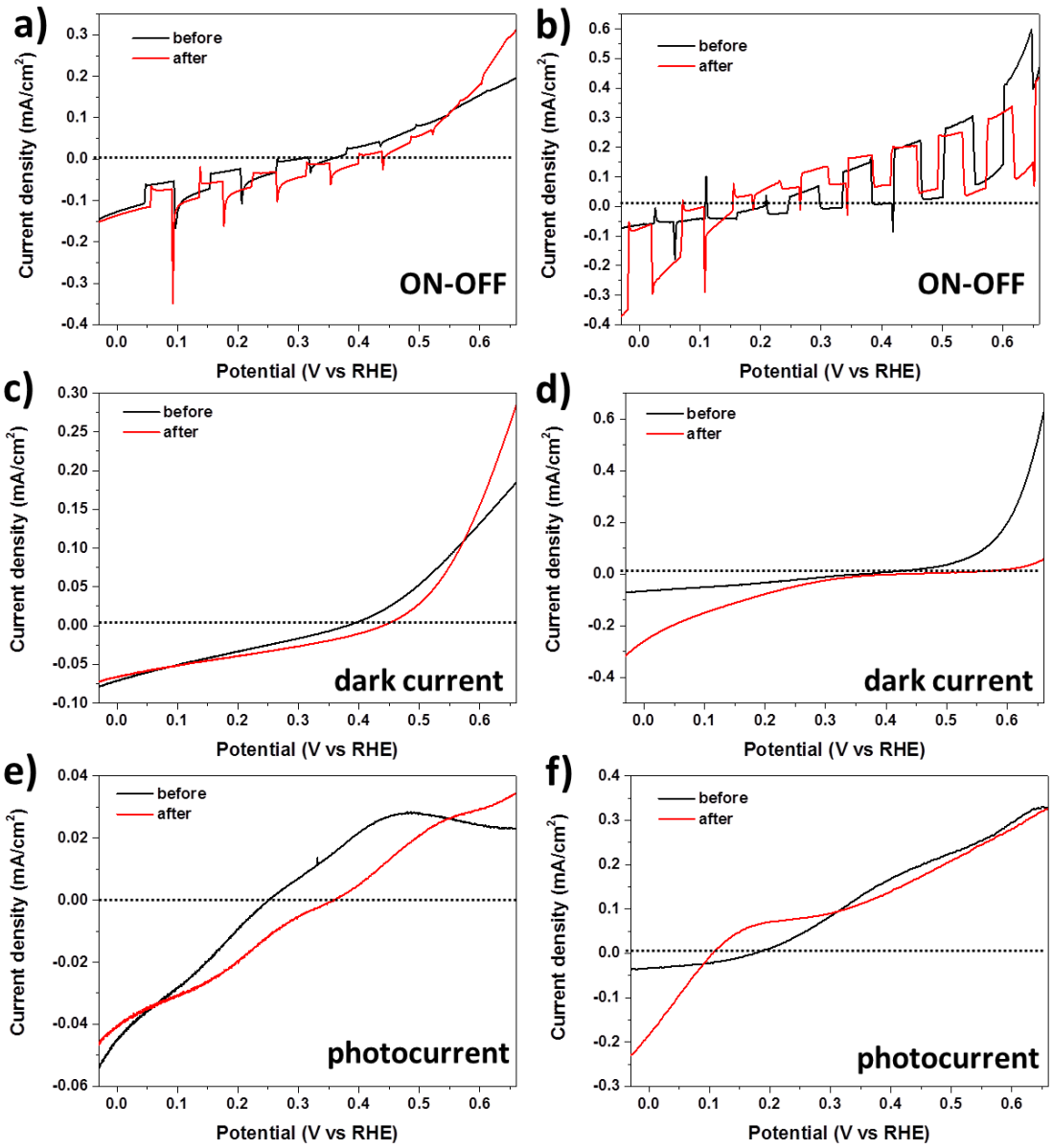

Figure 91. ON-OFF chopped illumination curves obtained for a) the bare GaAs NW array and b) the GaAs / TiO_2 / Pt NW array before (black) and after (red) the stability test; their corresponding c-d) dark current density and e-f) photocurrent density.

4. Conclusion

In this chapter, GaAs based NW array photoelectrodes were investigated for water splitting. We first optimized the GaAs NW core by adjusting the axial and radial growths by MBE. The exposed part of the substrate might serve as a back reflector improving the light absorption. Doped NWs were also investigated to improve the PEC performance by enhance the NW conductivity. But further studies are needed in order to figure out the doping concentration effect. Then a GaAs / $SrTiO_3$ NW array was fabricated with the procedure introduced in Chapter 5. Since a high structural quality for the interface and the oxide shell is

needed, the optimizing of GaAs / $SrTiO_3$ heterostructured NWs is still undergoing. Even though the first trial is failed, we still feel hopeful based on the success of the Si / $SrTiO_3$ hybrid system.[26] Besides, different GaAs / TiO_2 NWs were fabricated and characterized. The influences of the TiO_2 layer thickness and crystallinity on the PEC performances were studied. Thinner TiO_2 layer (less than 3 nm) is preferred. ALD is more suitable for this TiO_2 passivation layer deposition for more conformal and precise layer growth control. Then a Pt co-catalyst was introduced to the hybrid system to improve the water splitting efficiency. But the study on the TiO_2 layer and co-catalyst are far from enough, there are quite a lot of opening questions to be deal with. Even though the efficiency of the GaAs / oxide NWs based PEC cells is much lower than that for the wide band gap semiconductor systems, we can definitely improve it by optimizing the heterointerface structure, the passivation layer and the co-catalyst.

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Conclusion and perspectives

III-V semiconductor NWs have received much attention as a new class of materials with remarkable potentials for combining both advantages of III-V semiconductors with those of the nanoscale 1D geometry. The integration of functional oxides to III-V NWs is very promising due to the fact that oxides possess advantageous electric, thermal, and magnetic properties which most of semiconductors don't have. However, the study on this kind of heterogeneous structure is far from enough. This PhD work aims at developing the growth of GaAs (core) / oxide (shell) NW arrays on silicon substrates for photoelectrochemical water splitting. NWs were grown by MBE which offers a control of the structure and composition at atomic scale.

Firstly, the geometry and structure of the GaAs NWs were optimized by adjusting different experimental growth parameters during the self-catalyzed MBE growth. ZB GaAs NW arrays with good verticality were successfully grown on Si(111) substrates. The epitaxial relationship between the GaAs NWs and the Si(111) substrate was revealed through XRD measurements. With the help of *in-situ* RHEED measurements, the real time formation of the crystal phase of GaAs NWs was also studied.

We then systematically studied the surface oxidation of GaAs NWs and its negative effect on the subsequent shell growth. Our results highlight the benefit of the As-capping / decapping procedure for: i) protecting GaAs NWs against a surface oxidation/contamination induced by the air exposure and ii) achieving the growth of an epitaxial shell. This method could indeed serve as a general strategy for protecting the surface of III-V NWs therefore facilitating an epitaxial shell growth in various deposition reactors equipped with a heating sample holder. The growth of metallic, functional oxide or other semiconductor shell on III-V NWs with a controlled interface would then be possible.

Further we investigated the growth of a $SrTiO_3$ shell on self-catalyzed GaAs NW arrays. To control the growth of the $SrTiO_3$ shell, the GaAs NWs were protected via the As capping / decapping procedure in order to prevent uncontrolled oxidation and / or contamination of the NW facets. Thorough characterizations were done with the help of RHEED, SEM, TEM and XPS measurements. Using an adapted two-steps oxide growth method, it is shown that most of the perovskite $SrTiO_3$ shell appears to be oriented with respect to the ZB lattice of GaAs NWs. Hence the partial epitaxial growth of $SrTiO_3$ on {110}-type facets of GaAs NWs was obtained. The interface between the two kinds of material is however not abrupt and probably ascribed to prevent a perfect epitaxial growth all along the NW length. More studies might be done for the further interface structure optimization including the heating progress, the O_2 pressure control, *etc*. Through the thermal stability study, the GaAs / $SrTiO_3$

NWs show a good thermal resistance, which is positive for the further growth of functional oxides such as the ferroelectric $BaTiO_3$ oxide. These results are promising for achieving 1D epitaxial semiconductor (core) / functional oxide (shell) nanostructures even if more efforts should be done to fulfil the fully epitaxial growth of perovskite oxides on III-V NWs. Multifunctional devices coupling the outstanding properties of both core and shell materials might be certainly accomplished in the coming future.

The last part of this work concerns GaAs / oxide based NW arrays for PEC devices where the oxide serves as the passivation layer against the surface states as well as to protect the GaAs core from photocorrosion. The influence of the doping and morphology of the GaAs NWs was first studied. However further studies are needed to be carried out in order to figure out the doping concentration effect. We then studied on GaAs / $SrTiO_3$ NW arrays working as photoelectrode in PEC devices. The obtained results showed that the structural quality of partial epitaxial core / shell NWs is not sufficient for such applications. Since a high structural quality for the oxide shell and the GaAs/oxide interface is needed, the growth of GaAs / $SrTiO_3$ heterostructured NWs is now still under optimization. Thus, to avoid the degradation of GaAs NWs-based photoelectrodes, a TiO_2 passivation layer was applied either grown by MBE or by ALD. The effect of the thickness as well as the crystallinity of the TiO_2 layer was also investigated. Thinner TiO_2 layer (less than 3 nm) is preferred. ALD is a more suitable method for this TiO_2 passivation layer deposition due to a more conformal and precise layer growth control. Finally, co-catalyst Pt particles were introduced into the hybrid system to improve the water splitting performances. The studies on the TiO_2 layer and the Pt co-catalyst are however far from enough and there are quite a lot of opening questions to be deal with such as the size of the Pt particles and the contact between these Pt particles and the NW facet surface.

Appendix

1. Abbreviation

1D	one dimensional
2D	two dimensional
3D	three dimensional
NW	nanowire
APB	anti-phase boundary
VLS	vapor-liquid-solid
MBE	molecular beam epitaxy
ML	monolayer
BEP	beam equivalent pressure
ZB	Zinc Blende
WZ	Wurtzite
TPL	triple phase line
CMOS	complementary metal-oxide-semiconductor
CVD	chemical vapor deposition
MOCVD	metal organic chemical vapor deposition
PECVD	plasma enhanced chemical vapor deposition
PL	photoluminescence
RTA	rapid thermal annealing
PEC	photoelectrochemical
VB	valence band
CB	conduction band
SHE	standard hydrogen electrode

SCR	space charge region
UV	ultraviolet
UHV	ultra-high vacuum
RHEED	reflection high energy electron diffraction
TEM	transmission electron microscopy
HRTEM	high resolution TEM
SAED	selected area electron diffraction
EDX	electron energy dispersive X-ray spectrometer
XPS	X-ray photoelectron spectroscopy
KE	kinetic energy
BE	binding energy
IMFP	inelastic mean free path
RHE	reversible hydrogen electrode
STH	solar-to-hydrogen conversion efficiency
ABPE	applied bias photon to current conversion efficiency
APCE	absorbed photon to current conversion efficiency
IPCE	incident photon to current conversion efficiency
SC	semiconductor
RT	room temperature
SRV	surface recombination velocity
STEM	scanning transmission electron microscopy
SEM	scanning electron microscopy
HER	hydrogen evolution reaction
OER	oxygen evolution reaction
SCLJ	semiconductor / liquid junctions
ALD	atomic layer deposition

CT cell temperature

LSV linear sweep voltammetry

HAADF high angle annular dark field

EELS electron energy loss spectroscopy

2. Recipe of the sample fabrication

2.1. recipe for GaAs NW with radial growth

step name	time	general shutter	Ga cell temperature	Ga cell shutter	As cell temperature	As cracker temperature	As valve	sample holder temperature
cell preparation	00:00:10	off	e923 °C	off	e400 °C	e500 °C	p0%	e100 °C
	00:08:00	on						r385 °C
	00:02:00							e385 °C
predeposition of Ga	00:00:02			on				
	00:08:00		e945 °C	off				r450 °C
	00:02:00							e450 °C
	00:00:10						p19%	
NW axial growth	00:20:00			on				
	00:08:00		e923 °C	off			p25%	e340 °C
NW radial growth	00:20:00			on			p19%	
cooling	00:10:00			off			p0%	e100 °C
	00:00:10							

p : the percentage that the As valve is open;

e : the sample is heated to a given temperature directly;

r : the sample is heated to a given temperature progressively, the rate is the temperature difference devise the step time.

2.2. recipe for GaAs / $SrTiO_3$ NW

step name	time	general shutter	Sr cell temperature	Sr cell shutter	Ti cell temperature	Ti shutter	O partial pressure	sample holder temperature
preparation	00:10:00	off	555/435 °C	off	1522 °C	off	5E-8 Torr	e100 °C
	00:05:00							r250 °C
	00:01:00	off		on		on		e250 °C
first STO buffer layer	00:10:52	on						
annealing	00:15:00			off		off		r450 °C
second STO layer	00:10:52			on		on		e450 °C
cooling	00:10:00	off		off		off		e100 °C
	00:00:10						0 Torr	

2.3. recipe for GaAs / amorphous-TiO_2 NW

step name	time	general shutter	Ti cell temperature	Ti shutter	O partial pressure	sample holder temperature
preparation	00:10:00	off	1522 °C	off	5E-8 Torr	e100 °C
	00:01:00					r150 °C
	00:01:00	off		on		e150 °C
TiO_2 layer	00:22:44	on				
cooling	00:10:00	off		off		e100 °C
	00:00:10				0 Torr	

3. The effect of the substrate doping

To maximize the performance of the GaAs NWs based PEC cell, different types of Si(111) substrates were investigated, namely P-doped Si(111) ($10^{18}/cm^3$, labeled as n+), Be-doped Si (111) ($10^{16}/cm^3$, labeled as p) and Be-doped Si (111) with higher dopant concentration as $10^{18}/cm^3$ (labeled as p+). The PEC responses of these three types of substrates are shown in Figure 92. The n^+ Si(111) presents a very small contribution to the OER while the transient current is important which could be attributed to the slow reaction kinetics caused by the planar configuration of the Si substrate as discussed in Chapter 1.[1] The p^+ Si(111) shows the minimum transient current and barely contributes to neither the HER nor the OER. The p-type Si(111) slightly contributes to the HER and also suffers a slow kinetic. Since the PEC responses of all of the three substrates are negligible, we chose the p-type for its better resistance in the alkaline electrolyte.[2]

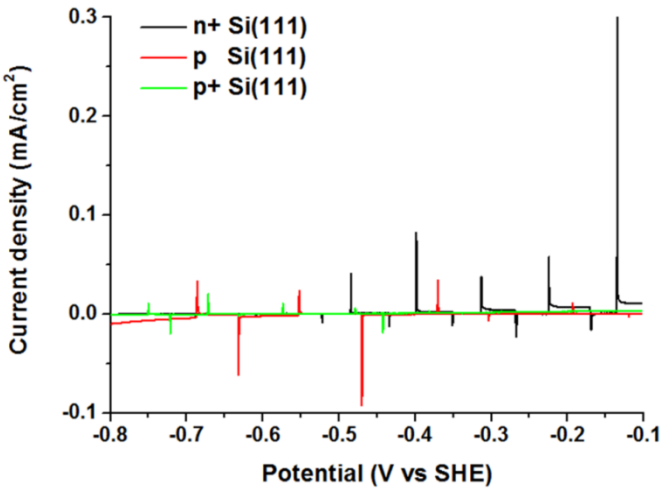

Figure 92. PEC performances of different Si(111) substrates.

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Résumé

Depuis 2004, lorsque le groupe de L. Samuelson a réalisé la croissance épitaxiale de nanofils (NFs) de semi-conducteur III-V sur un substrat de silicium (Si), l'intégration d'un semi-conducteur nanométrique à une dimension (1D) avec l'industrie très développée du Si s'est avérée permettre de fabriquer l'un des systèmes hybrides les plus prometteurs pour l'électronique et la photonique. Il existe deux manières de construire une hétérostructure avec d'autres types de matériaux tout en conservant la caractéristique 1D des NFs, à savoir les hétérostructures axiale et radiale (NF dit cœur-coquille). Il est ainsi devenu possible d'utiliser des NFs pour réaliser des nanostructures complexes permettant d'améliorer les performances des dispositifs électroniques et photoniques. Comparée à l'hétérostructure axiale, l'hétérostructure radiale a une tolérance plus élevée aux effets de surface. La géométrie cœur-coquille permet aussi une collecte plus efficace des porteurs de charge, ce qui est visé pour tous les dispositifs photoélectriques. Les NFs à hétérostructure radiale ont donc été préférés en raison des objectifs visés dans le cadre de cette thèse.

Jusqu'à présent, la plupart des travaux publiés sur les NFs cœur / coquille semi-conducteurs concernaient des semi-conducteurs de la même famille. La fabrication d'une coquille très hétérogène par rapport à un cœur semi-conducteur III-V d'un NF, tel qu'un oxyde fonctionnel ou un métal, représente donc un grand défi. L'une des difficultés provient de la procédure de croissance impliquant deux réacteurs d'épitaxie: pendant le transfert d'échantillons entre deux réacteurs séparés, les facettes du NF III-V subissent une oxydation et / ou une contamination incontrôlée. Une étude approfondie d'une telle oxydation et de son effet induit sur la croissance de la coquille ainsi que sur les propriétés de l'hétérostructure finale était manquante. Par ailleurs, une procédure permettant la protection des facettes des NFs, sans contamination et réversible, serait très utile pour la réalisation d'un dispositif à base de tels NFs hétérostructurés.

Récemment, l'intégration de matériaux hétérogènes tels que le silicium, des siliciures ou des métaux sur des NFs GaAs a été réalisée, ouvrant la voie à la fabrication de dispositifs originaux. Comme on le sait, les oxydes de type pérovskite ABO_3 possèdent un large éventail de propriétés, telles que la piézoélectricité, la ferroélectricité, *etc.*, complémentaires à celles des semi-conducteurs. Une telle combinaison permet ainsi le développement de dispositifs multifonctionnels. Jusqu'à présent, la combinaison avec semi-conducteurs avec des oxydes pérovskites n'a cependant été réalisée que pour des couches minces. Développer une méthode permettant la croissance épitaxiale d'une coquille d'oxyde pérovskite sur les NFs semi-conducteurs III-V est donc un objectif majeur à atteindre.

En ce qui concerne le problème écologique et la crise énergétique auxquels nous sommes confrontés, l'énergie récoltée à partir du rayonnement solaire offre une approche souhaitable. La production photoélectrochimique (PEC) d'hydrogène à partir de l'eau fournit un moyen de convertir directement l'énergie solaire en un combustible propre et stockable. Concernant l'énergie photovoltaïque, il est montré qu'une structure tandem combinant des semi-conducteurs ayant des bandes interdites différentes et complémentaires peut optimiser l'absorption du spectre solaire. Il est rapporté qu'une structure tandem, basée sur la combinaison d'un semi-conducteur III-V de bande interdite égale à 1,7 eV avec un substrat de Si de bande interdite égale à 1,1 eV, conduirait à une efficacité de conversion d'énergie optimale comparable à celle des cellules commerciales à triple jonctions. Plusieurs semi-conducteurs III-V ternaires ou quatrenaires satisfaisant une bande interdite de 1,7 eV peuvent être obtenus en ajustant leur composition (par exemple $Ga_{0,8}Al_{0,2}As$ ou $GaAs_{0,77}P_{0,23}$). Cependant, l'un des principaux problèmes qui empêche l'utilisation de tels semi-conducteurs III-V comme photocatalyseurs provient du fait que leurs surfaces sont photochimiquement instables dans un électrolyte. La réalisation d'une couche de passivation de ces semi-conducteurs adaptée à l'objectif PEC a donc attiré l'attention de la communauté des chercheurs. Concernant l'utilisation de NFs étudiée dans cette thèse, un réseau de NFs GaAs peut servir de système modèle pour démontrer la faisabilité d'une telle approche pour les applications PEC.

Cette thèse a donc visé à développer un réseau de NFs GaAs (cœur) / oxyde (coquille) pour le fractionnement de l'eau. La géométrie des NFs GaAs a été optimisée en ajustant différents paramètres expérimentaux de la croissance auto-catalysée de ces NFs par Epitaxie par Jets Moléculaires (EJM ou MBE en anglais pour Molecular Beam Epitaxy). Un réseau de NFs GaAs avec une bonne verticalité et une bonne qualité structurale a été fabriqué avec succès sur un substrat de Si(111). La relation d'épitaxie entre le substrat Si (111) et les NFs GaAs a été déterminée par des mesures de diffraction X (DRX). Avec l'aide de la diffraction RHEED *in situ* dans le réacteur MBE, la phase cristalline Zinc-Blende (ZB) ou Wurtzite (WZ) des NFs GaAs a pu être contrôlée.

Nous avons ensuite étudié systématiquement l'oxydation de surface des NFs GaAs et son effet négatif sur la croissance de la coquille. Les analyses mettent en évidence le bénéfice de la méthode dite d'encapsulation / désencapsulation arsenic (As), avec laquelle une couche d'As amorphe est déposée sur la surface des NFs GaAs pour: i) protéger les NFs GaAs contre l'oxydation de surface induite par l'exposition à l'air et ii) réaliser la croissance d'une coquille épitaxiale après la désorption de cette couche d'As amorphe. Cette méthode pourrait ainsi servir de stratégie générale de protection de la surface des NFs III-V, permettant la croissance épitaxiale d'une coquille hétérogène dans un réacteur d'épitaxie différent équipé d'un porte-échantillon chauffant. La croissance d'un oxyde métallique, d'un oxyde fonctionnel ou d'une autre coquille semi-conductrice sur des NFs III-V avec une interface contrôlée serait alors possible.

Nous avons ensuite étudié la croissance d'une coquille de $SrTiO_3$ sur des NFs de GaAs auto-catalysés. Pour contrôler la croissance de la coquille $SrTiO_3$, les NFs ont été protégés via la procédure d'encapsulation / désencapsulation As, afin d'empêcher une oxydation non contrôlée et / ou une contamination des facettes des NFs. Des caractérisations approfondies de la croissance de la coquille de $SrTiO_3$ sur les NFs de GaAs ont été réalisées à l'aide de mesures RHEED, SEM, TEM et XPS. En utilisant une méthode de croissance de $SrTiO_3$ en deux étapes, nous avons montré que la plus grande partie de la structure pérovskite $SrTiO_3$ était en relation d'épitaxie avec le réseau cristallin de GaAs. On obtient ainsi une croissance épitaxiale partielle de $SrTiO_3$ sur des NFs de GaAs. Grâce à une étude XPS de stabilité thermique réalisée au Synchrotron SOLEIL, nous avons montré que les NFs de GaAs / $SrTiO_3$ présentaient une bonne résistance thermique jusqu'à 500°C, ce qui est positif pour la croissance ultérieure d'une autre coquille d'oxyde fonctionnel tel que $BaTiO_3$ ferroélectrique. Ces résultats sont prometteurs pour la réalisation de nanostructures 1D semi-conducteur / oxyde fonctionnel. Des études supplémentaires devront cependant être effectuées pour réaliser la croissance épitaxiale parfaite de l'oxyde $SrTiO_3$ sur les NFs GaAs. Des dispositifs multifonctionnels couplant les propriétés complémentaires de matériaux de cœur et de matériaux de coquille pourraient ainsi être réalisés dans un futur proche.

La dernière partie de cette thèse concerne l'utilisation de tels réseaux de NF GaAs / oxyde pour les dispositifs PEC où l'oxyde sert de couche de passivation ainsi que de couche de protection des NFs GaAs contre la photocorrosion. L'influence du dopage et de la morphologie des NFs GaAs a d'abord été étudiée. Nous avons ensuite étudié les propriétés des réseaux de NFs de GaAs / $SrTiO_3$ servant de photoélectrodes dans des dispositifs PEC. Les résultats obtenus ont montré que la qualité structurale de ces NFs n'était pas suffisante pour de telles applications. L'optimisation de la croissance des NFs hétérostructurés GaAs / $SrTiO_3$ est actuellement en cours d'optimisation. Pour valider l'utilisation des photoélectrodes à base de NFs de GaAs, une couche de passivation de TiO_2 a été réalisée soit par croissance MBE soit par ALD (pour Atomic Layer Deposition). Les effets de l'épaisseur ainsi que de la cristallinité de la couche de TiO_2 ont été étudiés. Une couche de TiO_2 relativement mince (inférieure à 3 nm) s'est révélée préférable. L'ALD s'est aussi révélée une méthode plus appropriée que la MBE pour le dépôt de la couche de passivation TiO_2 en raison d'un contrôle plus précis de la croissance conduisant à une meilleure conformité. Finalement, des particules de platine (Pt) comme co-catalyseur ont été déposées sur les NFs GaAs / TiO_2 pour améliorer les performances de la photoélectrolyse de l'eau. Même si les résultats obtenus sont encourageants, ils sont cependant encore loin d'être suffisants et les études devront être poursuivies pour évaluer l'influence de certains paramètres comme, en particulier, la taille des nanoparticules de Pt et le contact entre ces particules de Pt et les facettes des NFs.

RESUME

L'objectif de cette thèse est de développer un réseau de nanofils GaAs (cœur) / oxyde (coquille) pour la photoélectrolyse de l'eau. Pour cela, la géométrie des nanofils GaAs a été d'abord optimisée en ajustant différents paramètres expérimentaux de la croissance auto-catalysée de ces nanofils par Epitaxie par Jets Moléculaires.

Nous avons ensuite étudié systématiquement l'oxydation de surface des nanofils GaAs et son effet négatif sur la croissance de la coquille. Nous avons donc développé une méthode dite d'encapsulation / désencapsulation d'une couche d'arsenic (As) amorphe qui protège les facettes des NFs de l'oxydation. Une étude physico-chimique a montré l'effet bénéfique d'une telle méthode sur la croissance de la coquille. La croissance d'une coquille de $SrTiO_3$ sur des nanofils de GaAs a ensuite été réalisée. Des caractérisations approfondies de la croissance de la coquille de $SrTiO_3$ sur les NFs de GaAs ont été réalisées. La plus grande partie de la structure pérovskite $SrTiO_3$ était en relation d'épitaxie avec le réseau cristallin de GaAs.

La dernière partie de cette thèse concerne l'utilisation de tels réseaux de nanofil GaAs / oxyde pour les dispositifs PEC où l'oxyde sert de couche de passivation. L'influence du dopage et de la morphologie des nanofils GaAs a d'abord été étudiée. Les propriétés des réseaux de nanofils de GaAs / $SrTiO_3$ et de GaAs / TiO_2 servant de photoélectrodes dans des dispositifs PEC sont étudiées.

ABSTRACT

The objective of this PhD is to develop the network of GaAs (core) / oxide (shell) nanowires for solar water splitting. The geometry of the GaAs nanowires was firstly optimized by adjusting different experimental parameters of the self-catalyzed growth of these nanowires by molecular beam epitaxy.

We then systematically studied the surface oxidation of the GaAs nanowires and its negative effect on the growth of the shell. We have therefore developed a method called the arsenic (As) capping / decapping method that protects the facets of nanowires from the oxidation. A physico-chemical study has shown the beneficial effect of such a method on the growth of the shell. The growth of a $SrTiO_3$ shell on GaAs nanowires was then performed. In-depth characterizations of $SrTiO_3$ shell growth on GaAs nanowires were carried out. Most of the $SrTiO_3$ perovskite structure was in epitaxial relationship with the GaAs crystalline lattice.

The last part of this thesis concerns the application of such GaAs / oxide nanowire networks to PEC devices where the oxide serves as a passivation layer. The influence of the doping and the morphology of GaAs nanowires was first studied. The properties of GaAs / $SrTiO_3$ and GaAs / TiO_2 nanowire networks used as photoelectrodes in PEC devices are finally studied.